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TECHNICAL OPERATING REPORT ON THE DATA INTEGRATION & COLLECTION ENVIRONMENT (DICE) INSTRUMENTATION SYSTEM DESIGN

WRIGHT LABORATORY

TRW
293 HIGHWAY 247 SOUTH
WARNER ROBINS GA 31088

SEP 1992

INTERIM REPORT FOR 05/01/91-08/30/92

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This technical report has been reviewed and is approved for publication.

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13. ABSTRACT (Maximum 200 words)

This Technical Operating Report (TOR) provides the top level and intermediate level hardware design of the DICE system. The design objectives are: 1) provide the capability to configure and control the collection of specific APG-63 radar and weapons system data, 2) provide for the collection of any and all D-bus, PMUX, CCMUX, and PACS communication data, 3) provide a data storage capability which exceeds two hours, 4) provide a mechanism for replaying the recorded data to the laboratory instrumentation data reduction and analysis system (IDRAS) in a time phased manner, 5) identify sources for dual compatible militarized and commercial off-the-shelf components, 6) provide prototype road map for the system's production, and 7) provide for filtered data capture processing.

Section 1 of this TOR presents a brief description of the overall objectives of this system. Section 2 identifies the applicable documents, both Government and non-Government, for the DICE system. Section 3 presents the instrumentation system design. Section 4 provides general information that aids in understanding this document (e.g., a list of acronyms and other abbreviations used herein).

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1 SCOPE

1.1 Identification

This Technical Operating Report (TOR), prepared in accordance with DI-S-30559/T, describes the instrumentation system design (ISD) identified as the Data Integration and Collection Environment (DICE) system. This report includes the top level and intermediate level system design information.

1.2 Background

The joint AFLC/AFSC Embedded Computer Resources Support Improvement Program (ESIP) is tasked to provide a means of providing reliable rapid radar system reprogramming capability. This capability will provide a means to perform software enhancements on current and future radar systems with significant reconfiguration of all fielded units within days. TRW's task is to develop a laboratory prototype of an on-board instrumentation system which is capable of collecting the useful data from the avionics radar system. The data collected by this system will aid analyst to perform reprogramming in a meaningful manner. The F-15 APG-63 radar is being utilized as the proof-of-concept for this system.

1.3 Document Overview

This TOR provides the top level and intermediate level hardware design of the DICE system. This report is structured in the following manner:

1) Section 1 presents a brief description of the overall objectives of this system.
2) Section 2 identifies the applicable documents, both Government and non-Government, for the DICE system.
3) Section 3 presents the instrumentation system design
4) Section 4 provides general information that aids in understanding this document (e.g., a list of acronyms and other abbreviations used herein).

2 REFERENCED DOCUMENTS

The following documents of the exact issue shown form a part of this document to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this document, the contents of this document shall be considered a superseding requirement.

Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the contracting agency or as directed by the contracting officer.

2.1 Government Documents

SPECIFICATIONS:

DI-S-30559/T 12 May 1989	Data Item Description, Technical Operating Report
MIL-E-5400T 16 November 1979.	Electronic Equipment, Aerospace General Specification

STANDARDS:

MIL-STD-461C 04 August 1986	Electromagnetic Emission And Susceptibility Requirements For The Control Of Electromagnetic Interference
MIL-STD-462 31 July 1967.	Electromagnetic Interference Characteristics, Measurement of
MIL-STD-810E 14 July 1989	Environmental Test Methods And Guidelines
MIL-STD-1472D 14 March 1989	Human Engineering Design Criteria For Military Systems Equipment And Facilities
MIL-STD-1553B 21 September 1978	Aircraft Internal Time Division Command/Response Multiplex Data Bus
MIL-STD-1788A 31 July 1989	Avionics Interface Design Standard
MIL-STD-2036 June 1991	General Requirements For Electronic Equipment Specifications 18 (COTS and Ruggedized Equipment Applications And Testing)

DRAWINGS:

NONE

OTHER PUBLICATIONS:

NONE

2.2 Non-Government Documents

SPECIFICATIONS:

7 May 1980	F-15 Instrumentation Interface Unit (IIU) Specification, Hughes Aircraft Corp.
H-009 12 March 1969	Multiplexer Bus System Specification, Mc Donnell Douglas Aircraft Corp.

STANDARDS:

None

DRAWINGS:

None

OTHER PUBLICATIONS:

F33615-87-C-1538	Radar Readiness Technology Report, Warner Robins Air Logistics Center
3173914-100	Programmable Signal Processor (PSP) Reference Manual
SD171500009-01 30 June 1989	Airborne Instrumentation Interface Unit System Manual, Comptek Research Inc.
26 October 1991	Single Function MIL-STD-1553B Interface Installation and User's Manual for VMEBUS Systems, SBS
421/HH/24620 Issue 2	PME CS/5 System Manual, Radstone Technology
HH681CPU3A	PMV 68 CPU-3A Manual, Radstone Technology
	PMV 68 CPU-3A Quick Start Guide, Radstone Technology
446/HH/67739 Issue 3	Radstone VIC068 Programming Manual, Radstone Technology
651/HH/19172/001 Issue 5	PLUM-4, Radstone Universal Monitor User Manual
AN104	PMV 68 Debug Port Adaptor Box
HH68102960	PMV 68 SCSI-1 Manual
421/HH/25653 Rev - 1 Issue 2	PMV VP-1 Manual

100010-007	ASM68K User's Guide, Microtec Research, Inc.
100009-008	ASM68K Reference Manual, Microtec Research, Inc.
100008-008	ASM68K Installation Guide, Microtec Research, Inc.
November 1990	DOS to 680x0 Cross-Compilation, System User Manual, Alsys, Inc.
March 1989	386 DOS Compiler User Manual, Alsys, Inc.
February 1989	DOS Ada Compiler Ada Developer's Toolset, Volume 1, Alsys, Inc.
January 1983	Ada Reference Manual, Alsys, Inc.
	MC68030 Enhanced 32-Bit Microprocessor User's Manual, Third Edition, Motorola Rev. 2
	M68000 Family Programmer's Reference Manual, Motorola
	MS DOS 5.0 User's Guide and Reference Manual
December 1990	EXB-8500 8mm Cartridge Tape Subsystem Product Specification, EXABYTE Corporation
08 April 1991	EXB-8500 8mm Cartridge Tape Subsystem User's Manual, EXABYTE Corporation

3 DICE SYSTEM DESIGN

3.1 Design Criteria

The following paragraphs describe the design criteria for the basic laboratory prototype of the DICE system. The design for the flight version is not addressed in this document.

3.1.1 Design Objectives

The DICE system is designed to meet or exceed the following criteria:

1) Provide the capability to configure and control the collection of specific APG-63 radar and weapons system data.
2) Provide for the collection of any and all D-Bus, PMUX, CCMUX, and PACS communication data.
3) Provide a data storage capability which exceeds two hours.
4) Provide a mechanism for replaying the recorded data to the laboratory instrumentation data reduction and analysis system (IDRAS) in a time phased manner.
5) Identify sources for dual compatible militarized and commercial-off-the-shelf components (COTS).
6) Provide prototype road map for the system's production.
7) Provide for filtered data capture processing (Smart Record Option).

3.1.2 System Definition

The laboratory DICE system is a Motorola 68030 25 MHz, VME based system utilizing a custom programmable hardware interface which operates under the control of operational software written in Ada. The system uses the commercial version of the RADSTONE CPU3A militarized processor. The data storage system consists of the EXABYTE EXB-8500 8mm cartridge tape subsystem. The programmable hardware interface design utilizes Xilinx field programmable gate array (FPGA) logic. Figure 3-1 provides a top level view of the laboratory DICE system.

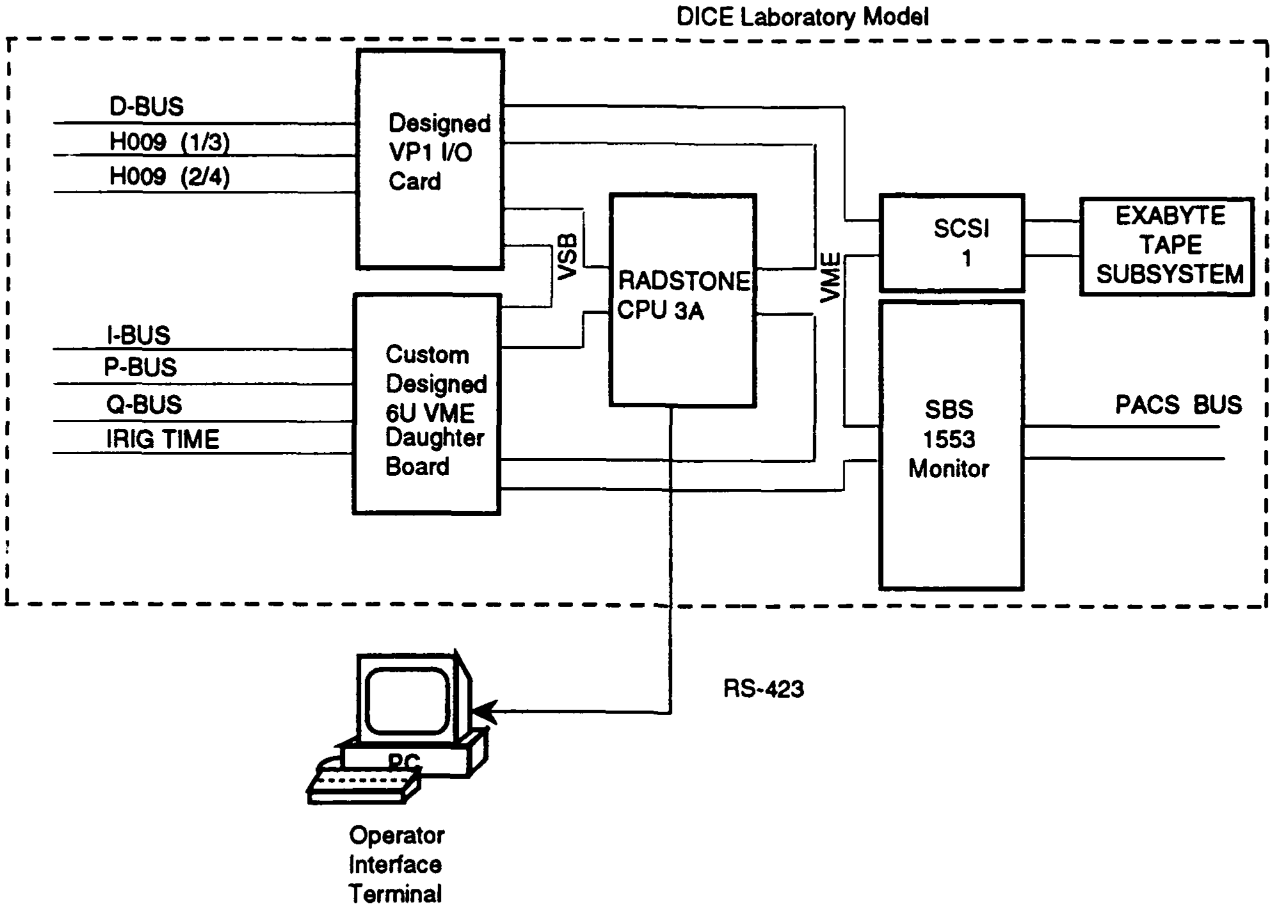

Figure 3-1. DICE Laboratory System Diagram

3.1.3 Data Volumes and Rates

After laboratory level analysis of the target systems medium pulse repetition frequency (MPRF) Track Mode data transmissions, the following data rates and volumes have been established as a minimum load capability for the DICE system.

Table 3-1. Data Volume and Rate Criteria

SOURCE	WORD COUNT	WORD SIZE(bytes)	TRANSMISSION RATES(Hz)	VOLUME (Bytes/Sec)
D-BUS	1024	3072	97.7	300,134
P-BUS	16	48	97.7	4,690
Q-BUS	16	48	97.7	4,690
I-BUS	15	45	97.7	4,396
H009 1/3	211	422	20.0	8,440
H009 2/4	283	596	20.0	11,320
Total Volume Rate				333,670

The DICE system has an initial throughput rate of 1 Mbyte/sec. Based on the target systems data rates and volume, the DICE system has an aggregate (software and hardware) utilization of 34% with the remaining 65% available for future growth. The DICE system is designed with flexibility and growth in mind. The hardware design allows for technology insertion and easier system retargetting. The data storage and data transfer capacity can be increased by incorporating enhanced versions of the current components [1]. The software for the basic system utilizes less than 20% of the available processor resources providing adequate growth for future needs.

3.1.4 Smart Record Option Design Criteria

The smart record option (SRO) of the DICE system provides a means of selectively recording data base upon pre-defined filtering criteria. The intent of the SRO is to increase the amount of significant data recorded thus increasing the operational time of the system without changing the recording hardware. The smart record option allows for two levels of data recording.

1) Open - All data is recorded. Default and override.

2) Intelligent - Only certain message groups are collected, filtered and recorded. Hardware configuration and software filters.

The SRO DICE system will use event triggers to initiate and suspend the data recording. The SRO DICE system will use the P-MUX Radar Data Processor (RDP) Mode Word as the primary source for trigger information. The D-Bus, P-Bus, Q-Bus, H009, I-Bus and Weapons Bus data are recorded when the P-MUX RDP Mode Word indicates that the radar is in:

1) Target Acquisition Mode

2) Target Track Mode

3) Burst Ranging Mode

In all cases the SRO DICE system will monitor and hold buffers containing 10 seconds of search mode data to be recorded when the radar mode switches from search mode to one of the three trigger modes. Additionally, 10 seconds of search mode data is recorded after the radar mode has been reset to search mode.

3.2 Operational Design

The DICE system is defined to consist of three operations; collection definition, data record, and data playback. The DICE system is designed to perform data recording in either a laboratory or aircraft environment. The playback and collection definition operations are laboratory only modes. The DICE system performs real-time data recording, non-real-time off-line data collection and real-time playback. Figure 3-2 shows the DICE system's states and transitions.

The following paragraphs describe the functional operation of each of the DICE system's operational modes.

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[1] The enhanced versions of these components (tape unit and interface system) will not be available until mid-1993.

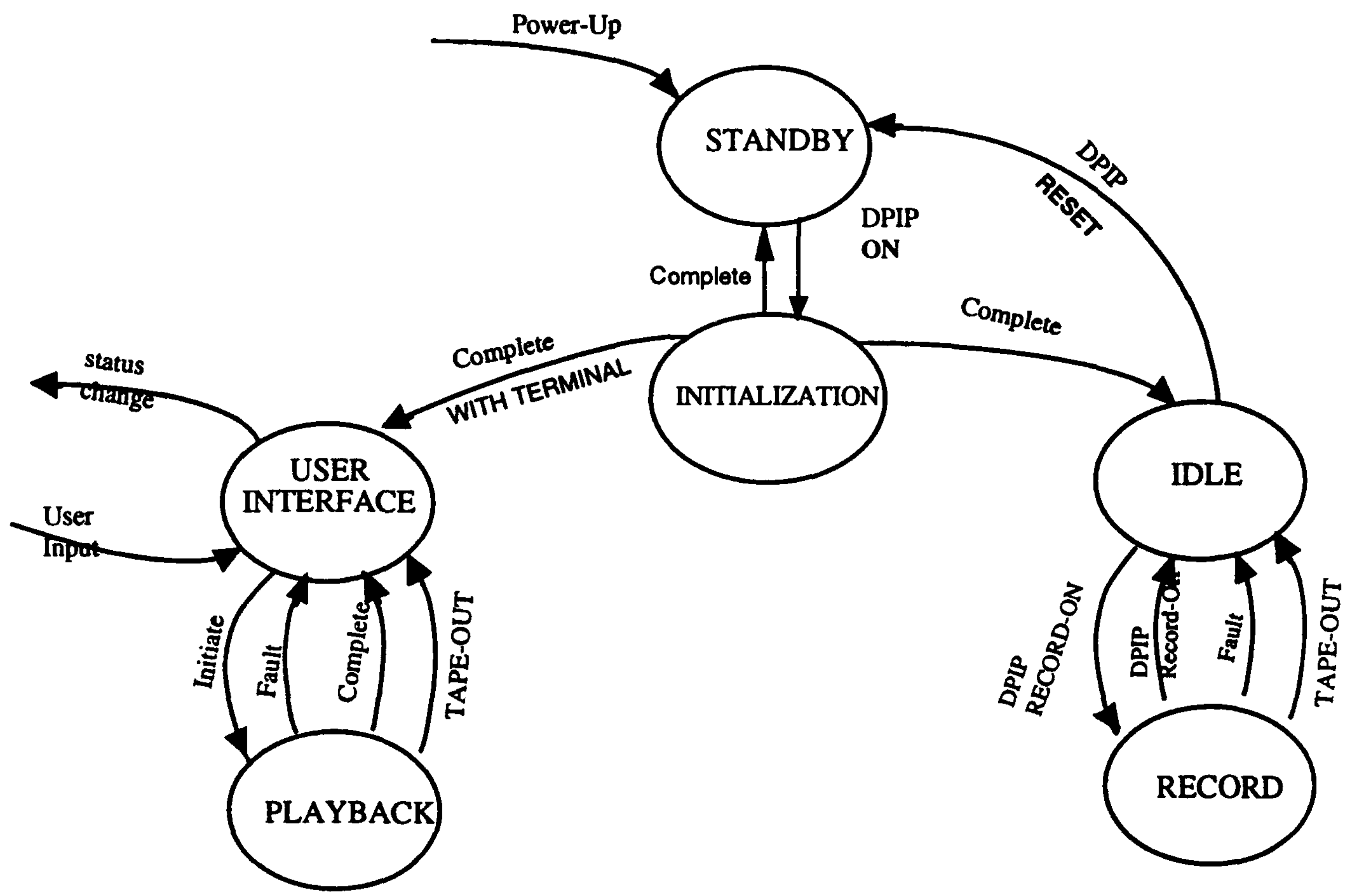


Figure 3-2. DICE System Top Level State Transition

3.2.1 Collection Definition

The user, using a off-line PC system, can define the hardware configuration and collection criteria for the DICE system. The user may define his collection in terms of:

1)	D-Bus (1 - 6)	(yes/no)	Default = yes
2)	I-Bus	(yes/no)	
3)	P-Bus	(yes/no)	
4)	Q-Bus	(yes/no)	
5)	PACS	(yes/no)	
6)	H009 (1/3)	(yes/no)	

a) Air Data Computer (ADC)
b) Attitude Heading Reference Set (AHRS)
c) Heads-up Display (HUD)

d) Lead Computer Gyro (LCG)
e) Navigation Control Indicator Panel (NCI Panel)
f) Radar Warning Receiver (RWR)
g) Internal Countermeasures Set (ICS)

7) H009 (2/4) (yes/no)

a) Horizontal Situation Indicator (HSI)
b) Inertial Measurement Unit (IMU)
c) Life History Recorder (LHS)
d) Radar
e) Vertical Situation Display (VSD)

8) Radar Data Processor mode

a) Target Acquisition
b) Target Track
c) Burst Ranging
d) Target Acquisition/Target Track
e) Target Acquisition/Burst Ranging
f) Target Track/Burst Ranging
g) All

3.2.2 Record Operation

The DICE system becomes operational when power is applied, either laboratory or aircraft. However, *the DICE system is not initialized until the operator depresses* the "ON" button of the Dice Pilot Interface Panel (DPIP). The DPIP is discussed further in Section 3.3.2.3. At that time, the DICE system hardware is initialized and system software is loaded and initialized. If the "ON" signal is dropped, the DICE system ceases operation. If "ON" is re-initiated the system is reinitialized and all previous data is lost. The system must be "ON" for recording or playback. The system is placed in IDLE mode until recording is requested.

After the DICE system is activated, "ON", the operator can pseudo-synchronize the digital data with the video data by depressing the "RECORD" button. This interrupts the DICE software's idle loop and causes the data collection initiation per the predefined collection criteria. The operator may suspend collection by depressing the "RECORD" button again. This will drop the signal and cause an interrupt which signals the DICE software to change states back to IDLE.

During the "RECORD" operation, the operator may choose to override the predefined collection criteria. Depressing the "OVERRIDE" button causes an interrupt in the DICE software. The override flag is set and all bus data is collected until the override is terminated. The termination of the override is initiated by the operator depressing the OVERRIDE button again.

The operator has the ability to perform a "soft reset" of the DICE system. The soft reset dumps all currently held non-recorded data, resets the hardware configuration to the smart configuration, performs BIT, places a reset marker on the tape, and continues the recording from that point. The reset occurs when the operator depresses the RESET button on the DPIP.

The DPIP has three LEDs which indicate the health status of the DICE system. The red FAULT LED is illuminated whenever a fault is detected in the DICE system. This light may clear during a "RESET" or "ON" operation. The yellow TAPE-OUT LED indicates that all of the available tape has been used. The DICE system transitions to the IDLE state at this point. When data is written to the

tape unit the white "DATA RECORDED" LED is illuminated. It remains lit until the DICE "ON" button is depressed for initialization.

3.2.3 Playback Operation

After the DICE Laboratory system is powered up, the operational software will determine whether or not a console unit is attached to the system. If a console is present, the DICE operational software will enter the interactive user interface mode.

At this point, the user selects the time frame desired for playback. The time tolerance is 0.000 secs to 15960.000 seconds. The DICE tape system is advanced to the time selected. Data is transferred from the tape system to processor memory in 5K word blocks. The hardware is configured to the transmit mode and the data is replayed in the order in which it was recorded, based on time.

When the stop time or end of tape is reached control is returned to the operator. In the playback operational mode, the operator may not use the DPIP functions. The DPIP status lights are also active during playback.

3.3 Hardware Design

The DICE system uses field programmable gate array (FPGA) logic to define I/O interfaces. This allows for dynamic, on-line, software controlled reconfiguration of the interface definition. Using this mechanism, the DICE system affords the test engineer the ability to select which buses are to be monitored.

3.3.1 Interface Control Design Criteria

The DICE data collection hardware interfaces to the host via VMEbus. There are three VME addressable registers which provide mode control, configuration control and system status. The control register provides the capability to set the mode of the system (record, playback, or BIT). It also controls which buses are to be enabled for data recording or playback and when to start and stop data collection.

The configuration register is used only during the initilization phase. This initialization occurs at power up and for each mode change (i.e. change from record to playback mode). This register is VME addressable and provides the path by which configuration data is downloaded to the Xilinx FPGA devices.

The status register is a read-only VME addressable register which provides the host with DICE system status. This status includes handshaking signals needed during hardware configuration, BIT faults, etc..

3.3.1.1 Timing Diagrams

Figure 3-3 represents target system waveforms that are to be recorded and played back in the laboratory. Figure 3-4 represents the D-Bus data synchronization and blocking scheme. Figure 3-5 represents the inter-range instrumentation group (IRIG) B time code format. Figure 3-6 depicts the PCM waveforms of the target system.

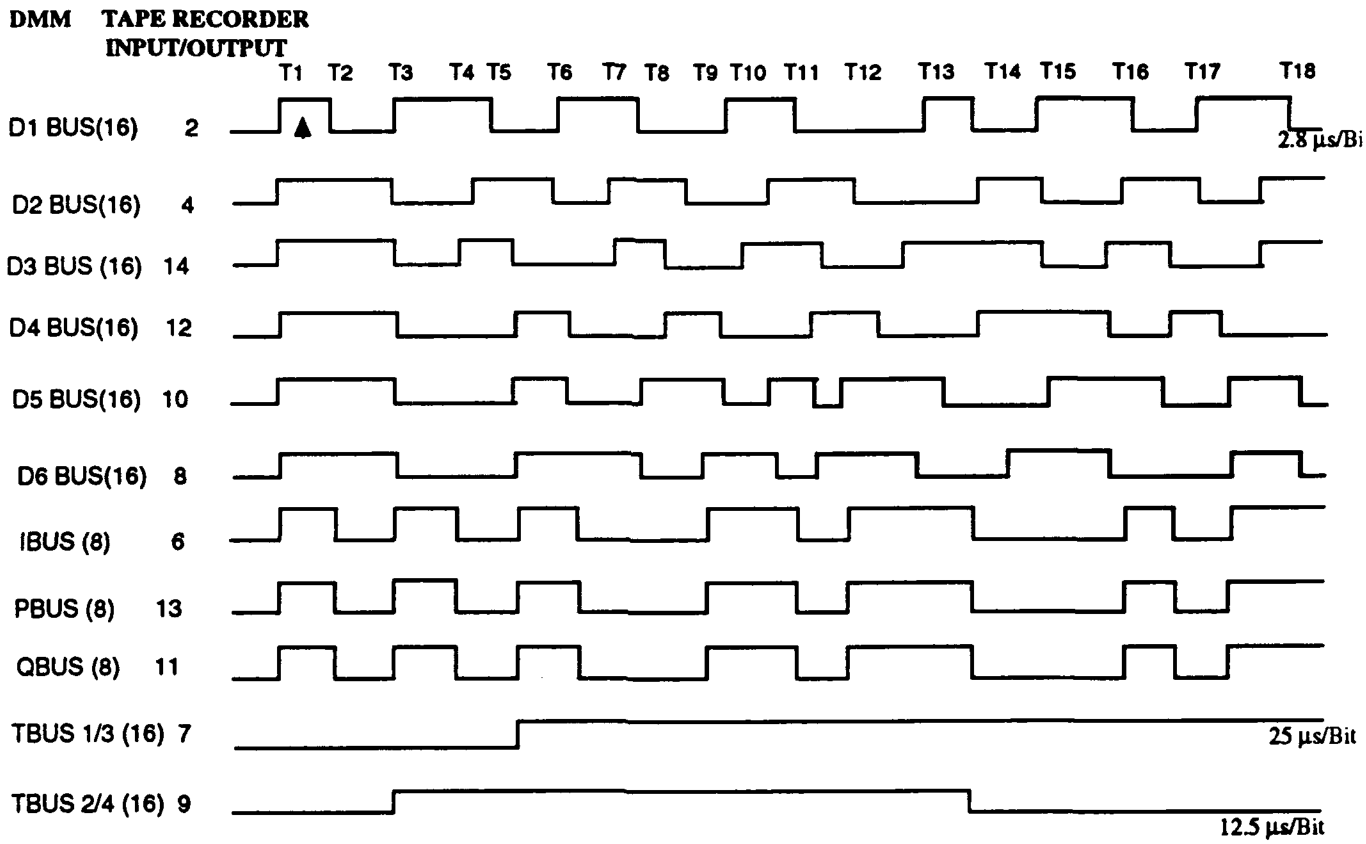


Figure 3-3. Target System Waveform Timing Diagram

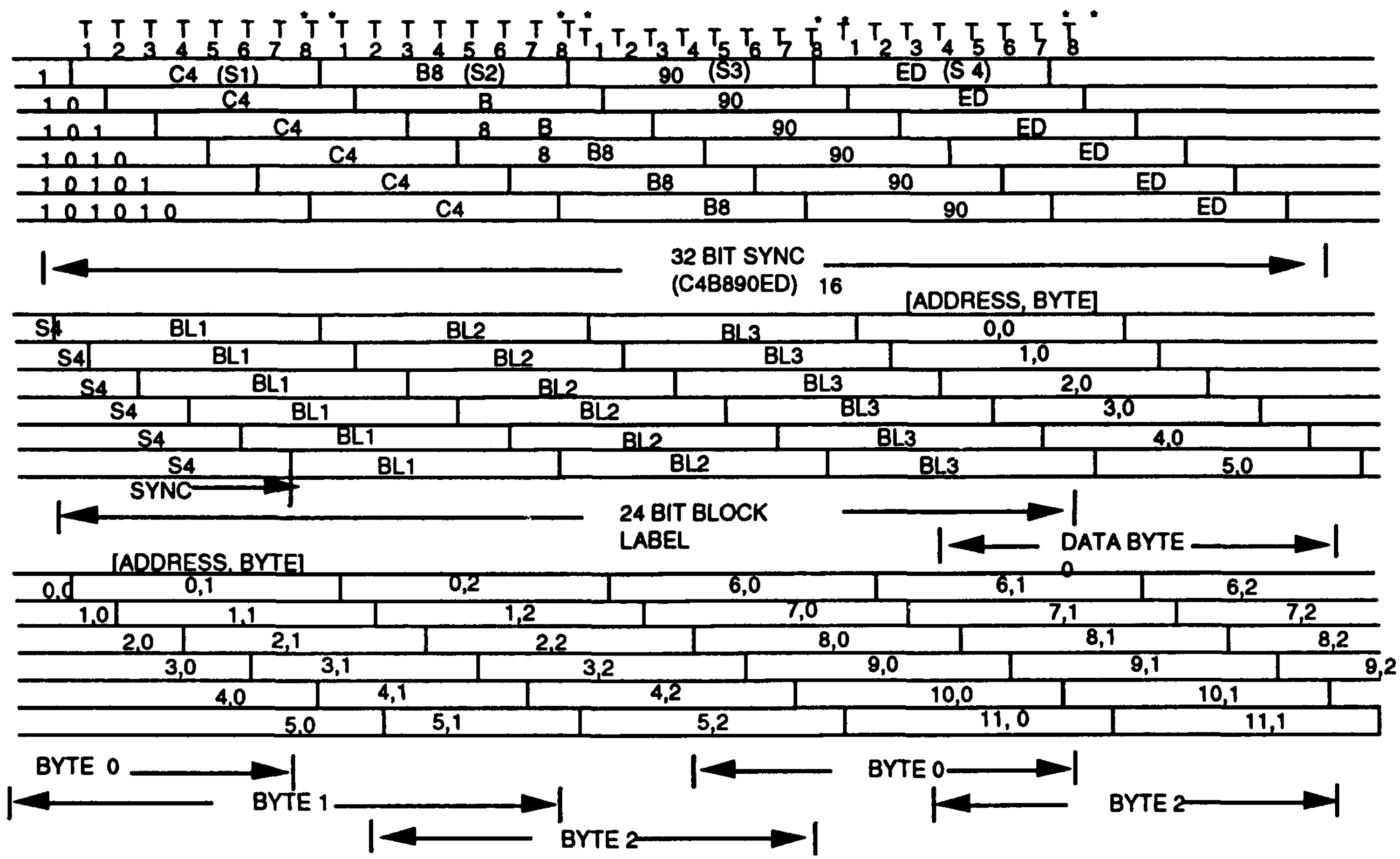


Figure 3-4. D-Bus Data Synchronization and Blocking

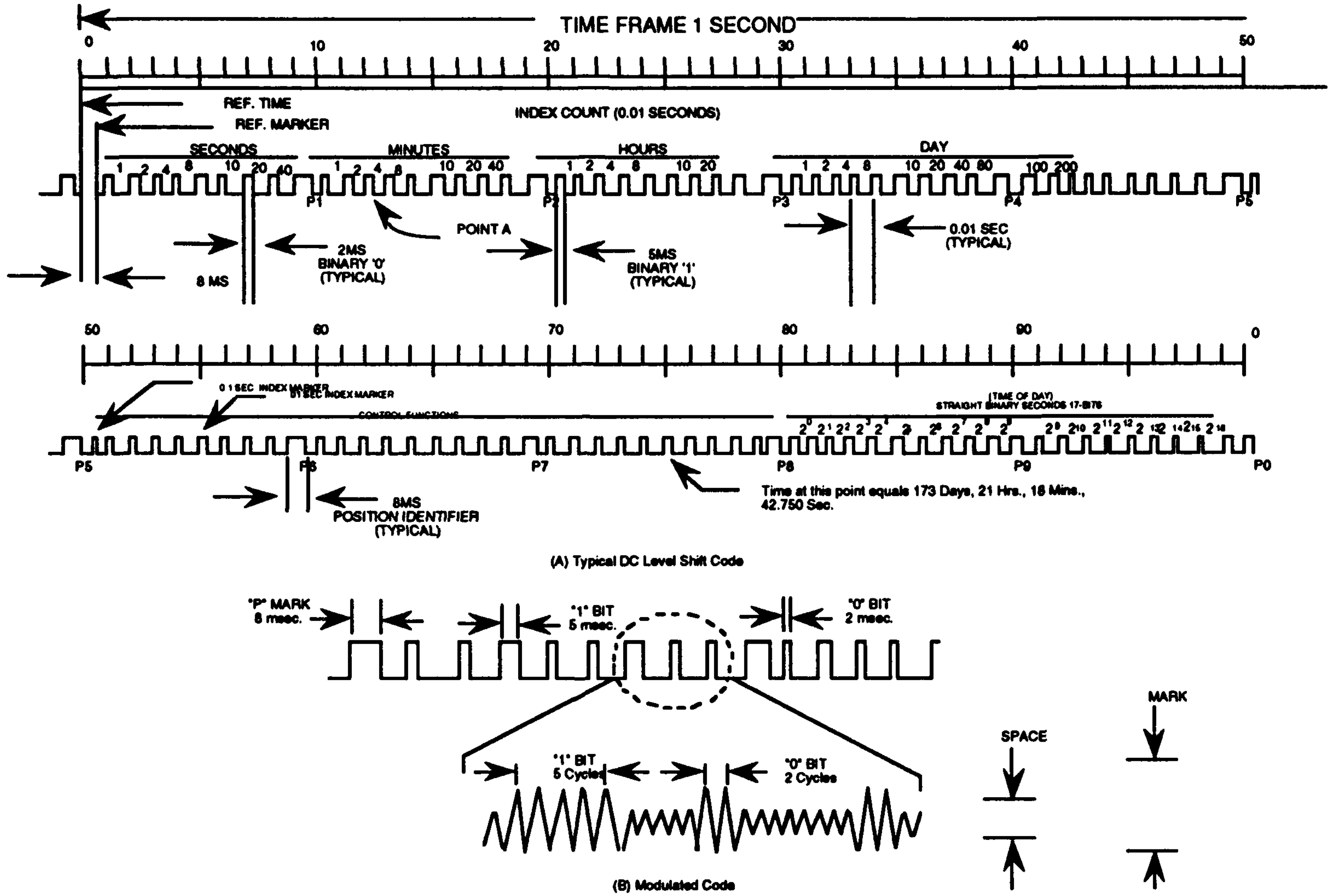


Figure 3-5. IRIG B Time Code Format

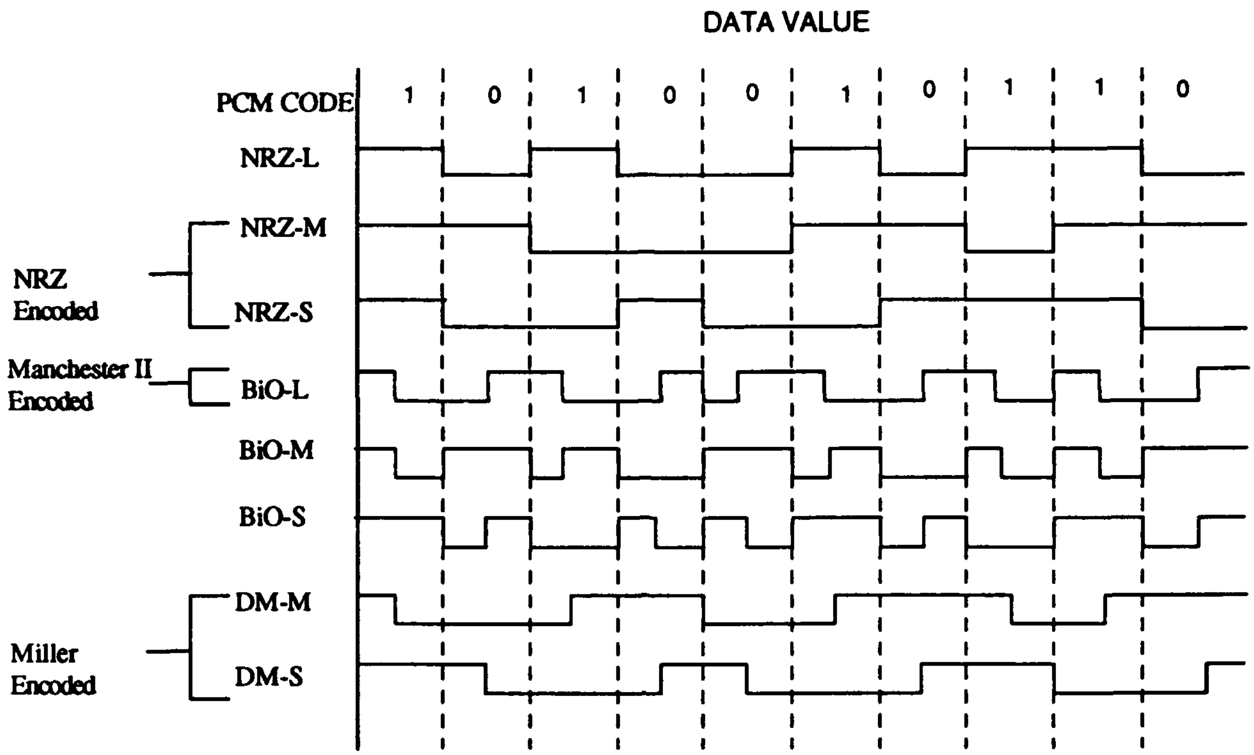


Figure 3-6. PCM Waveforms Diagram

3.3.1.2 PCM Codes

The following describes the pulse code modulation (PCM) codes utilized within the DICE system:

BIPhase-L [2]: A change in level occurs at the center of each bit period

"1" Is represented by a level during the first half of the bit period.
"0" Is represented by a level which is negative with respect to a "1" during the first half of the bit period.

DM-M [3]:

"1" Is represented by a level change at the center of the bit period.
"0" Is represented by another level change at the beginning of the bit period EXCEPT when the bit is preceded by a "1" in which case no level change occurs during the bit period.

2 BIPhase-L is also referred to as MANCHESTER II. It is the encoding scheme used by H-009 MUXBUS and the 1553 WEAPONS BUS.

3 DM-M is also referred to as MILLER CODE. It is the encoding scheme used by the IIU as a direct input to the analog tape.

3.3.2 Mechanical Design

3.3.2.1 Laboratory Configuration

The mechanical design of the DICE laboratory prototype is an aggregate of the COTS devices. The custom designed hardware will be housed in the VME chassis.

Figure 3-7 represents the DICE system control box. The unit is a COTS VME chassis with five printed circuit board (PCB) slots. The I/O connectors to the laboratory IDRAS patch panel and the RS-432 operator terminal are located on the right side of the user space. The DICE system is configured as follows:

Slot 1:	RADSTONE CPU3A card
Slot 2:	VP1 Custom I/O Control card
Slot 3:	VME Custom I/O Card
Slot 4:	Small Computer Serial Interface (SCSI) card
Slot 5:	MIL-STD-1553B Bus Monitor card

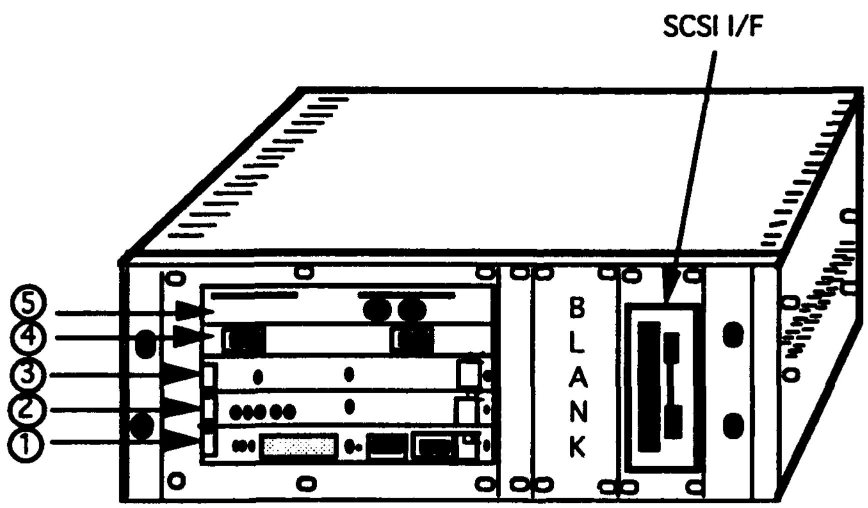


Figure 3-7. DICE Laboratory System

Figure 3-8 gives the external dimension of the EXABYTE EXB-8500 tape cartridge system. This unit will be connected to the control box via cable to the SCSI controller.

3.3.2.2 Airborne Configuration

The airborne configuration of the DICE system is TBD when Option 2 is executed.

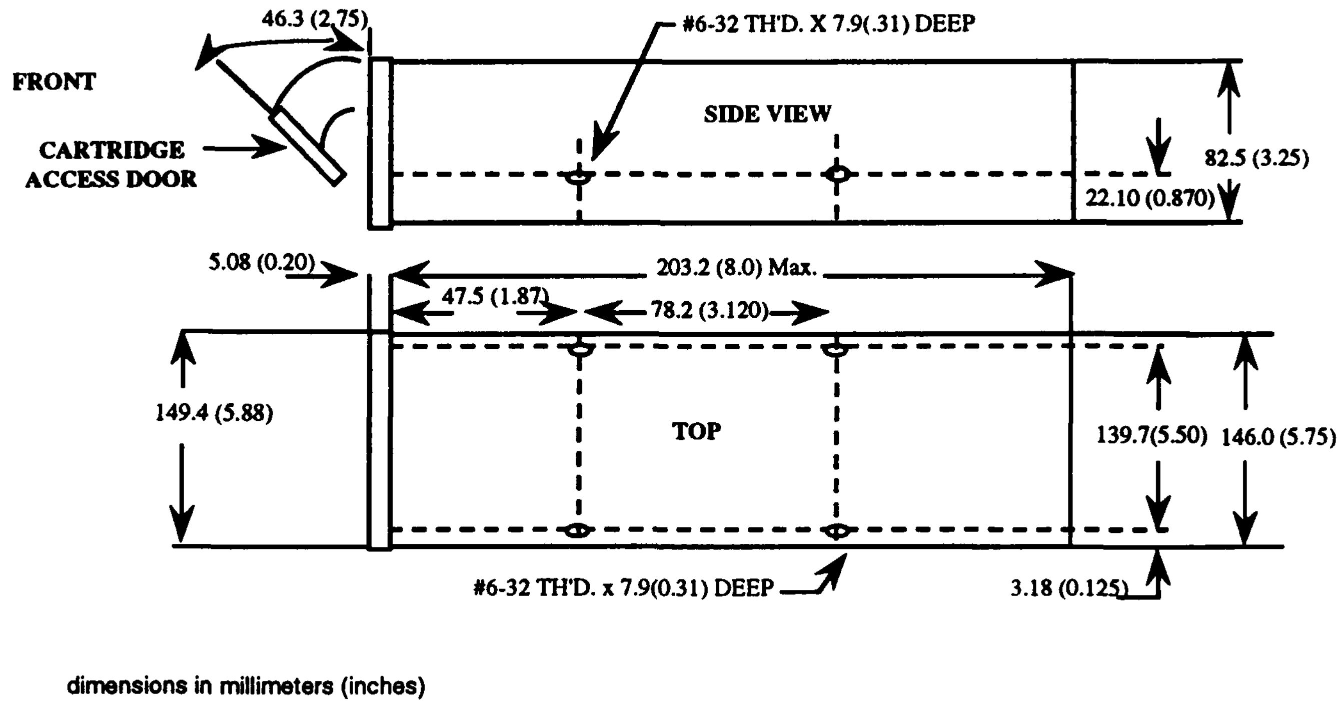


Figure 3-8. EXABYTE EXB-8500 Dimensions

Figure 3-9 represents the VP1 I/O development card which receives the data signals from the IDRAS patch panel, synchronizes with the words and messages, packs the data into 32 bit VME words, ID tags each VME word and interrupts the CPU for transfer via the VSB bus. The shaded area labeled "user area" is approximately 40 in^2. FPGA circuitry is used to execute the necessary configuration operations. The remaining portion of the PCB is populated with circuitry necessary to operate the VME communications and an 8 bit processor used to perform initialization and configuration.

3.3.2.3 DICE Activation Mechanism

The SRO DICE system is activated using the DICE Pilot Interface Panel. This panel allows the pilot to activate, control and monitor the DICE System. The laboratory prototype will be instrumented to utilize this mechanism. The DPIP consists of four back-lit, spring latched buttons and two LEDs.

The "ON" button is a locking alternating function button protected from accidental depression by a clear hinged cover. This button's function shall be viewed as an initialize/standby mode. When active this button is back lit white.

The "RECORD" button is a locking alternating function button. This button starts and suspends the data recording operations. The "RECORD" button is back lit green.

The "OVERRIDE" button is a locking alternating function button which notifies the DICE system that all data is to be recorded, thus overriding the smart record function. The "OVERRIDE" button is backlit orange.

The "RESET" button is a momentary function button which notifies the DICE system that a soft reset should be performed. The "RESET" button is back lit yellow.

The red "FAULT" LED is activated whenever an error in the DICE system is detected. A "hard" or "soft" reset may clear this indicator.

The yellow "TAPE-OUT" LED is activated when all available tape has been used.

The white "DATA RECORDED" LED is activated whenever data has been written to the tape. Figure 3-10 depicts the DPIP.

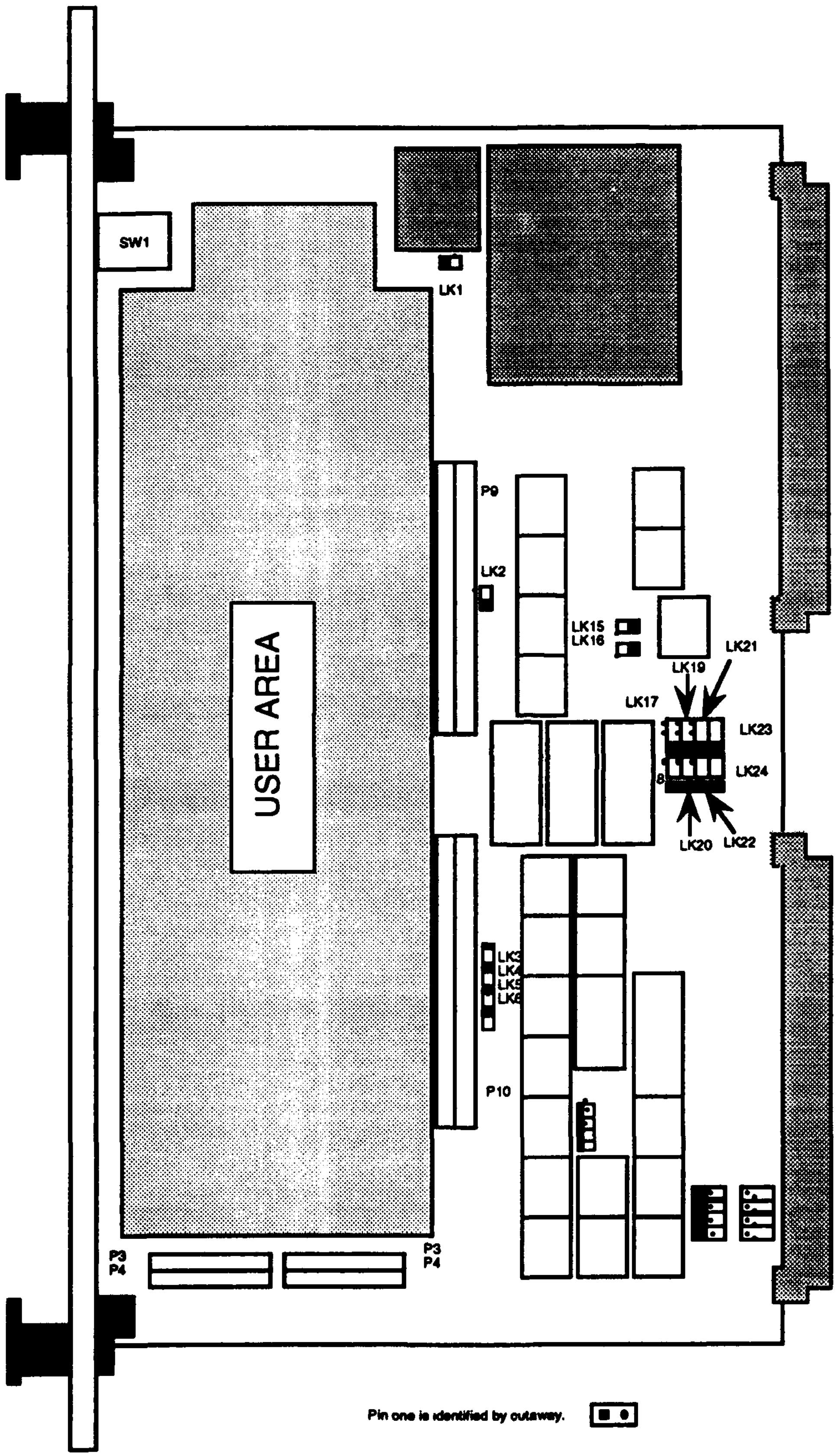


Figure 3-9. VP1 VME Development PCB

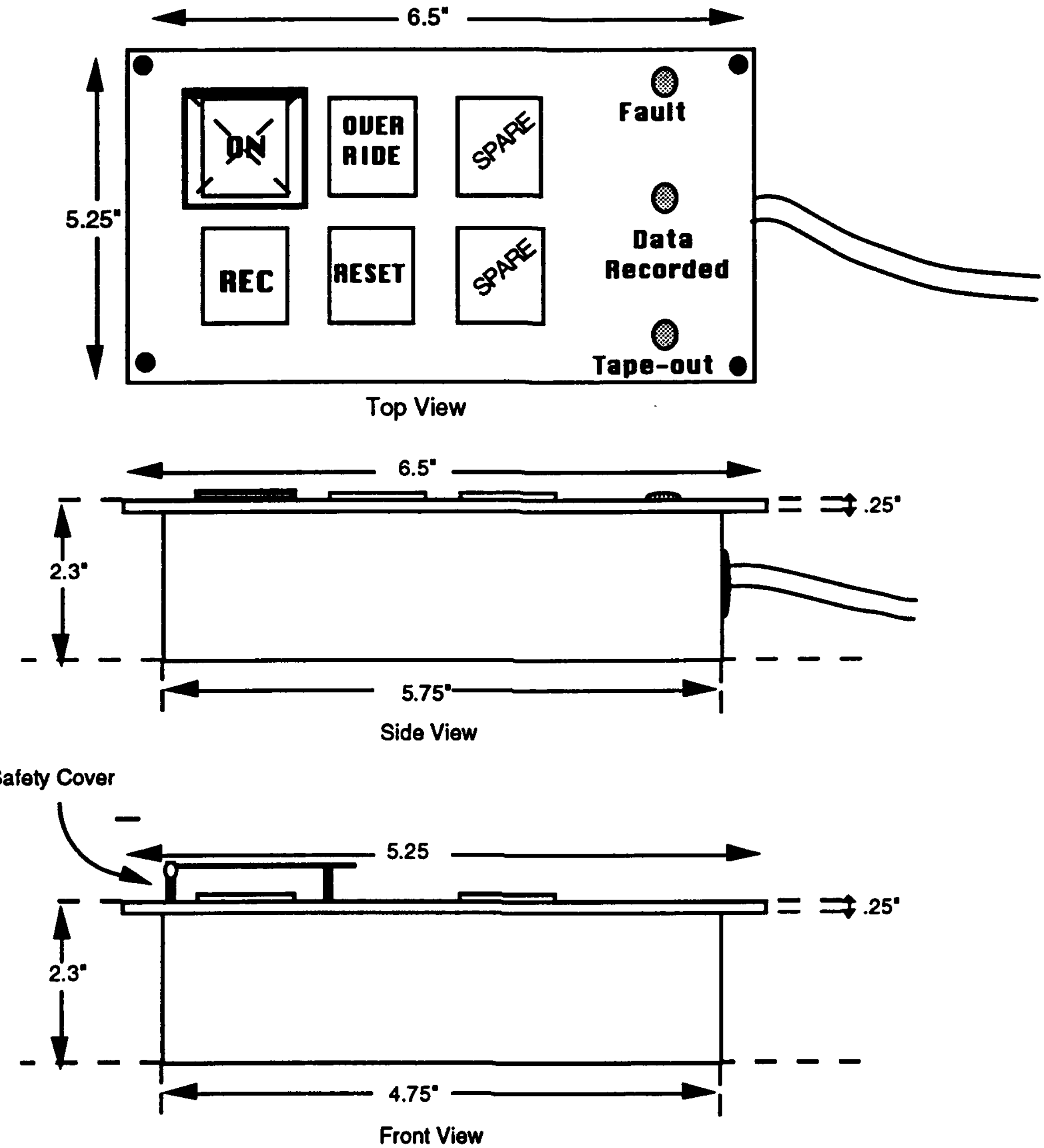


Figure 3-10. DICE Pilot Interface Panel

3.3.3 Electrical Design

The DICE data collection system is implemented on a Radstone VP1 I/O card with a second VME type card piggy-back as a daughter board. This design will require two VME slots. The VP1 I/O Card contains a Radstone provided VME interface and a prototype area to be used for DICE hardware. The

logic contained on this board includes a TRW designed VSB interface, all registers needed to interface to the host system and buffering for inter-board signals.

The daughter board contains the target interfaces and is necessary due to space constraints caused by the number of data collection channels. This board gets power and ground from the VME backplane but does not require a separate slow address. To alleviate space constraints all target interfaces are implemented using Xilinx FPGA's. These devices are dynamically reprogrammable so that different logic functions can be implemented using the same hardware.

The complete schematic circuitry design for the VP1 I/O card is not complete for the draft ISD document. Figures 3-11 and 3-12 represent a portion of the VP1 card logic at a top level. Appendix A contains the circuit board detailed block diagrams and the VPI preliminary schematics.

3.3.3.1 Data Source Pinouts

In the DICE laboratory demonstration system, the central computer multiplexer (CCMUX) connections signals have been converted to NRZ 0 to +5vdc. These signals are available at the IDRAS patch panel and will be accessed by using a BNC "T" connector at each signal cable patch point.

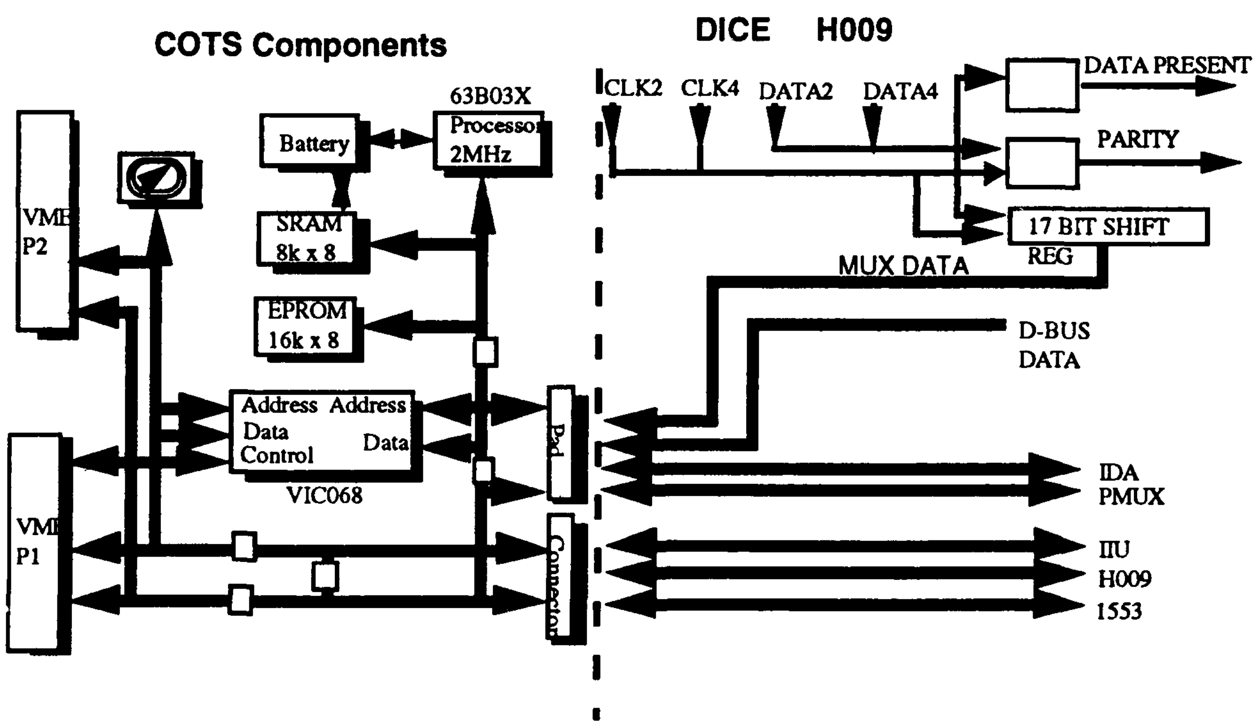


Figure 3-11. Top Level DICE H009 and IIU Interface Logic

3.3.3.2 Circuit Board Layout

Appendix A of this report provides the detailed block diagram for the DICE hardware and the schematics.

3.3.3.3 EMI/EMC Considerations

The question of EMI/EMC effects and the DICE system is as yet unanswered. Under the basic DICE program, the laboratory prototype is unable to provide any insight in this area. Only with the flight worthy model can this issue be addressed. However, through careful selection of COTS components which have a low EMI/EMC characteristics for the laboratory prototype, the airborne version should subsequently have a low EMI/EMC profile.

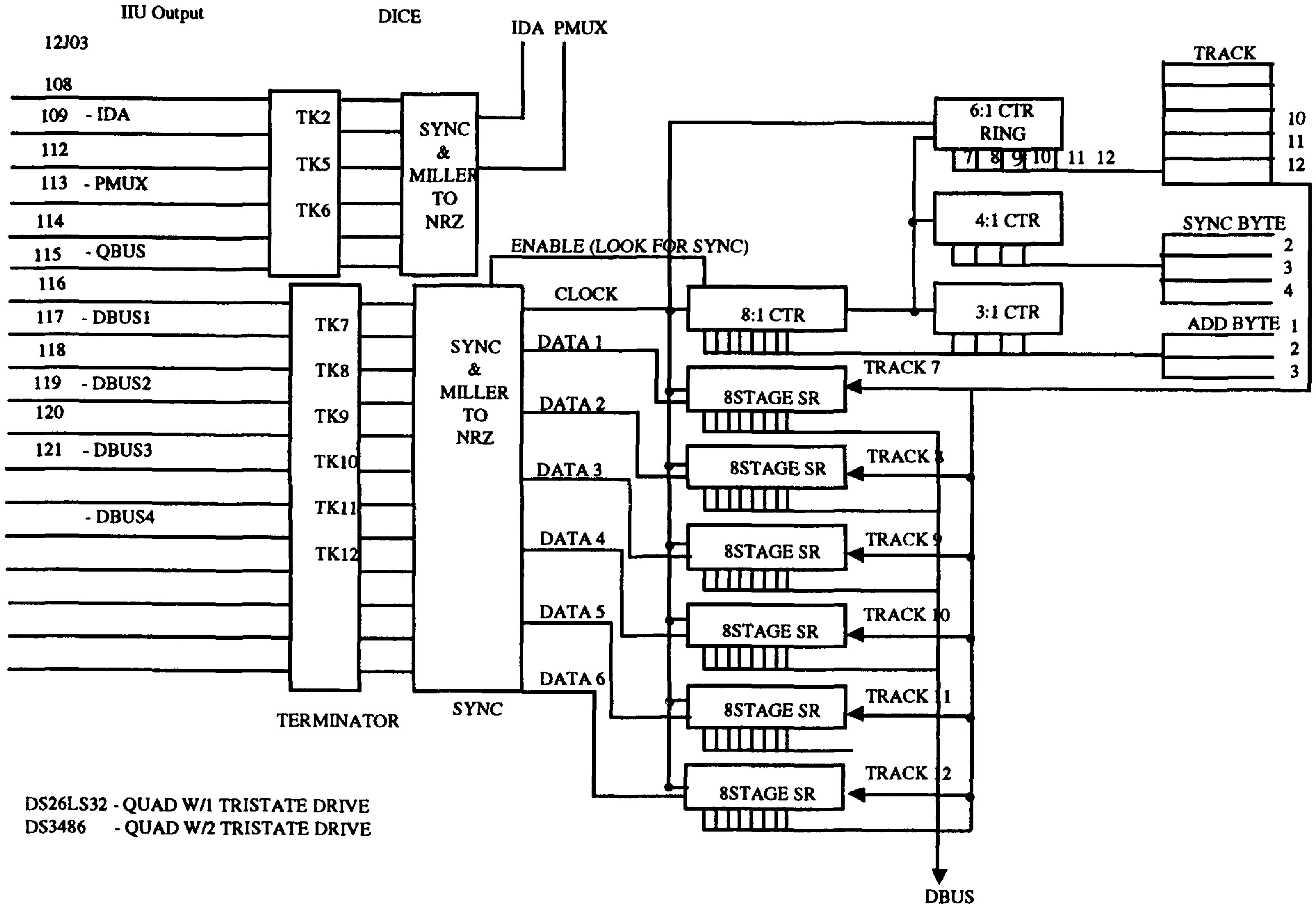


Figure 3-12. Detailed DICE H009 and IIU Interface Logic

3.4 Software Design

The DICE software configuration item (CSCI) consists of four computer software components (CSC). Each CSC is written in Ada. The CSCI is designed to perform both the data record and data replay functions of the DICE system. The DICE software is divided into two functional parts, the DICE Bootstrap Executive and the DICE System software (OFP - operational flight program). The DICE Bootstrap Executive is in firmware in the CPU3A card itself while the DICE OFP is downloaded from the EXABYTE tape system. This configuration allows for dynamic reconfiguration of the collection criteria and system configuration. The following paragraphs describe the function of each CSC. Figure 3-13 provides a top level view of the DICE software CSCI.

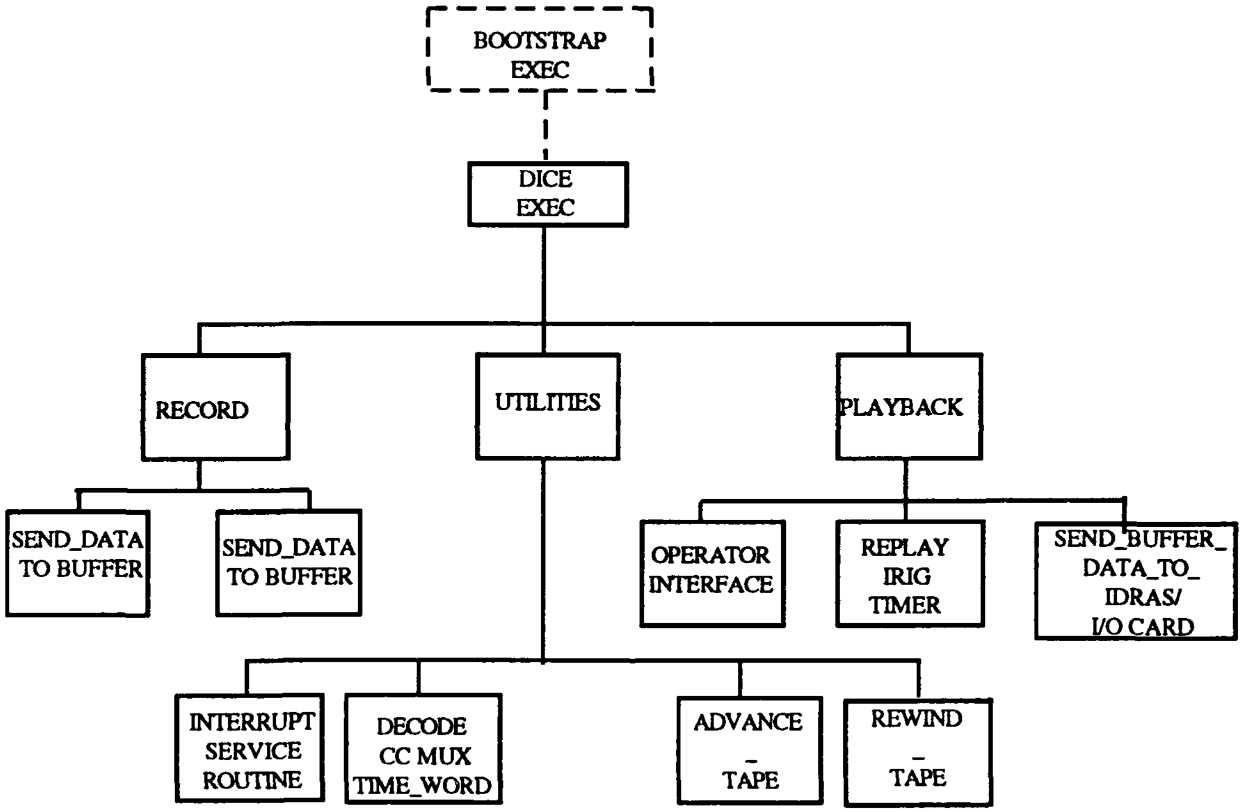


Figure 3-13. DICE CSCI Top Level Diagram

Table 3-2 provides the processing time and memory allocation budgets for the basic DICE system software.

Table 3-2. DICE Software Timing and Memory Allocations

CSC/DATA AREA	*Memory Budget (Bytes)	Allocated Processing Time	Max. Lines Of Executable Code
DICE EXECUTIVE CSC	360	860 µSEC	30
BIT CSC	240	240 µSEC	20
DECODE TIME WORD CSC	300	300 µSEC	25
OPERATOR INTERFACE CSC	600	600 µSEC	50
ADVANCE TAPE CSC	120	133000 mSEC	10
REWIND TAPE CSC	120	133000 mSEC	10
SEND BUFFER DATA CSC	300	.0918 SEC	25
RECEIVE DATA TO BUFFER CSC	300	.0918 SEC	25
BOOTSTRAP EXEC CSC	120	120 µSEC	10
INTERRUPT SERVICE ROUTINE CSC	600	600 µSEC	50
IRIG TIMER CSC	600	600 µSEC	50
SMART PROCESS CSC	300	.0918 SEC	25
DATA BUFFER	6144	N/A	N/A
LOCAL DATA	205	N/A	N/A
TOTAL	10,309	266.279 SEC	330

3.4.1 Bootstrap Executive

The Bootstrap Executive (BSX) CSC performs all of the necessary startup functions required to initiate the DICE system. The BSX is programmed into the user area of the CPU3A EPROM, where its functionality remains constant. At power up the Bootstrap Executive performs master processor built-in-test(BIT) and peripheral BIT. The BSX sets the appropriate status lights on the DICE control box and DPIP when BIT results are negative. After successful startup, the BSX, utilizing the EXABYTE tape system, loads the DICE OFP into the CPU3A's RAM for execution. The BSX then transfers execution control to the DICE Executive CSC for operational functions. Figure 3-14 provides a state transition diagram for the DICE system.

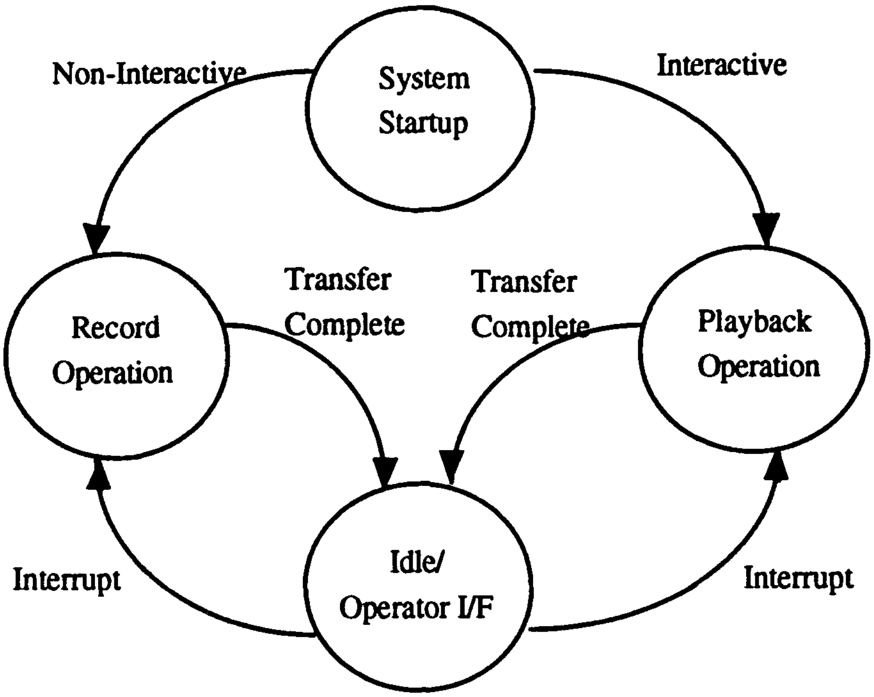


Figure 3-14. DICE State Diagram

3.4.2 DICE Executive

The DICE Executive (DEX) CSC provides control for the DICE system during operation. The DEX monitors all BIT reports and arbitrates control between the Record and Playback CSCs. The DEX determines the operational mode of the system and establishes the initial hardware configuration for the DICE system. Figure 3-15 depicts the processing flow of the DEX.

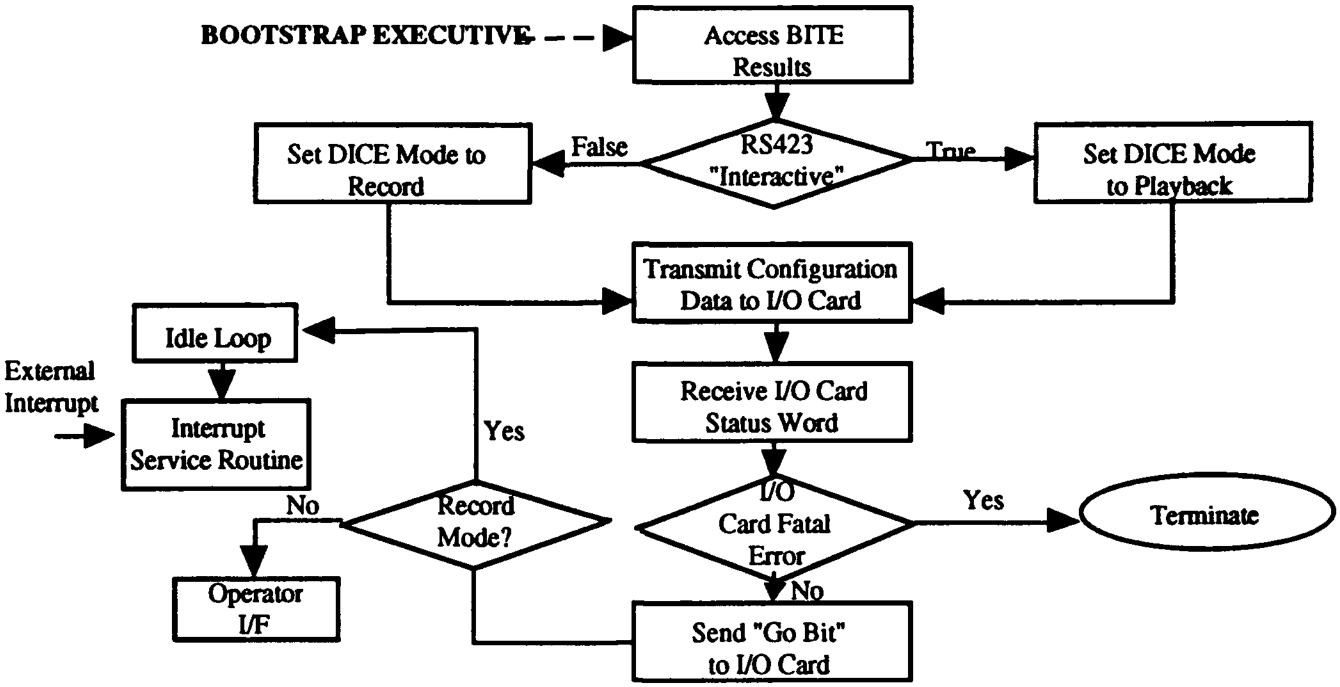


Figure 3-15. DICE Executive Processing Flow Diagram

3.4.3 DICE Record

The DICE Record CSC performs the data collection screening (Smart Record) and recording functions of the DICE system. DICE Record accepts the captured data from the VP1 I/O and 1553 monitor cards, and prepares it for storage on the EXABYTE tape system. Under the Smart Record option, the DICE Record CSC will perform criteria checks on the captured data to ensure that only the requested data is recorded. The DICE Record will also establish the control for reconfiguring the hardware, as necessary, for the Smart Record.

3.4.4 DICE Playback

The DICE Playback CSC performs the data playback function of the DICE system. DICE Playback accepts user specified start and stop times to control the transmission of recorded data. The DICE Playback provides the configuration control to setup the VP1 I/O 1553 monitor/control cards to transmit the data to the IDRAS patch panel.

4 TEST PLANS

The following paragraphs describe the test methodology which will be used to ensure that the DICE system is functionally and operationally correct.

4.1 Hardware Test Plans

The DICE COTS hardware components will be tested for functionality based upon the advertised capabilities. Defects and departures from the stated capabilities will be noted and evaluated as to impact on the system design. The vendor will be challenged to explain and correct discrepancies prior to the component in question inclusion into the DICE system. If the vendor cannot correct a problem or demonstrate a work around, another source will be selected.

The DICE custom I/O card hardware configuration item (HWCI) will undergo three levels of testing to ensure functionality.

1) Logic Simulation testing. Utilizing CAD/CAE logic design tools, the designed circuitry logic will be simulated to test functionality of the design and correctness of components prior to being sent to PCB layout.

2) Board level testing. Using logic analyzers and other laboratory test equipment, the custom PCB will be tested for signals, rates, power, connectivity, and other crucial areas prior to hardware integration testing.

3) Integration Testing. Integration testing will consist of integrating the custom PCB and other hardware components to verify communications and control processing.

4.2 Software Test Plans

The DICE system software is to be developed in accordance with TRW's approved and accepted software development practices and procedures. The DICE CSCI will undergo five levels of testing and evaluation to ensure functionality and correctness.

1) Design Walk-throughs. The DICE CSCI design will be reviewed by the system engineer for functional, structural, and logical correctness prior to code and test.

2) Low Level Testing. Each low level software module or unit (CSU) will be tested during the code and unit test phase. Testing will consist of syntactical correctness, processing logic flows, data handling and exception handling.

3) Unit Level Testing. After each CSU of a CSC has passed unit level testing, the CSUs are integrated and tested. Testing consists of control flow checks, data communication, and functionality.

4) Control Testing. Each CSU/CSC which provides control for hardware within the DICE system is tested with the hardware for functionality. This testing is done in conjunction with the hardware engineer to resolve anomalies.

5) CSCI integration Testing. Each tested CSC is incorporated into the CSCI and tested for control flow and communications. Once this testing has been successfully completed, the CSCI is baselined.

4.3 System Integration Test Plans

After the DICE HWCI, COTS hardware and CSCI components have completed their respective testing, The system will be tested as a whole. System integration testing will utilize the advanced radar test bench system (ARTBS) located in the F-15 avionics integrated support facility (AISF) in Building 227 at Robins AFB GA. The integration test will be conducted as follows:

1) DICE system connected to the ARTBS through proper interfaces.

2) A known test scenario will be run on the ARTBS with both the DICE system and the laboratory recording device on. The test will be a minimum of five minutes.

3) The laboratory recorded data will be run through the IDRAS and a analysis report generated.

4) The DICE system will be configured to the replay mode and the recorded data transmitted to the IDRAS and an analysis report will be generated.

5) The two reports will be compared and anomalies identified and classified. The laboratory data is considered to be reliable and accurate.

These five steps will be repeated a minimum of six times (three test with one scenario, and three using a different known scenario). Any discrepancies will be reviewed and analyzed. Should changes be necessary to the DICE HWCI or CSCI, the changes will be submitted to a configuration control board (CCB) for review and evaluation. The CCB will consist of government and contractor personnel.

5 NOTES

5.1 Acronyms

AFLC	Air Force Logistics Command
AFSC	Air Force Systems Command
AISF	Avionics Integrated Support Facility
ARTBS	Advanced Radar Test Bench System
BSX	Bootstrap Executive
CCB	Configuration Control Board
CCMUX	Central Computer Multiplexer
COTS	Commercial-Off-The-Shelf
CSC	Computer Software Component
CSCI	Computer Software Configuration Item
CSU	Computer Software Unit
DEX	DICE Executive
DICE	Data Integration and Collection Environment
DPIP	DICE Pilot Interface Panel
EMC	Electromagnetic Characteristics
EMI	Electromagnetic Interference
ESIP	Embedded Computer Resources Support Improvement Program
FPGA	Field Programmable Gate Array
HWCI	Hardware Configuration Item
IDRAS	Instrumentation Data Reduction and Analysis System
IIU	Instrumentation Interface Unit.
ISD	Instrumentation System Design
PACS	Programmable Armament Control System
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
MPRF	Medium Pulse Repetition Frequency
OFP	Operational Flight Program
RDP	Radar Data Processor
SCSI	Small Computer Serial Interface
SRO	Smart Record Option
TBD	To Be Determined
TOR	Technical Operating Report

10 DETAILED HARDWARE DESIGN

The following pages represent the to-date detailed hardware design for the DICE Laboratory prototype.

Figure 10-1 represents the top level hardware interconnects for the DICE I/O control boards.

Figure 10-2 represents the block layout of the RADSTONE VP1 development board.

Figure 10-3 represents the block layout of the custom 6U VME daughter board.

Figure 10-4 provides a detailed block level view of a single channel process.

Figure 10-5 (8 pages) provides the actual schematics for the VPI I/O.

Further design details are TBD until the prototype is completed.

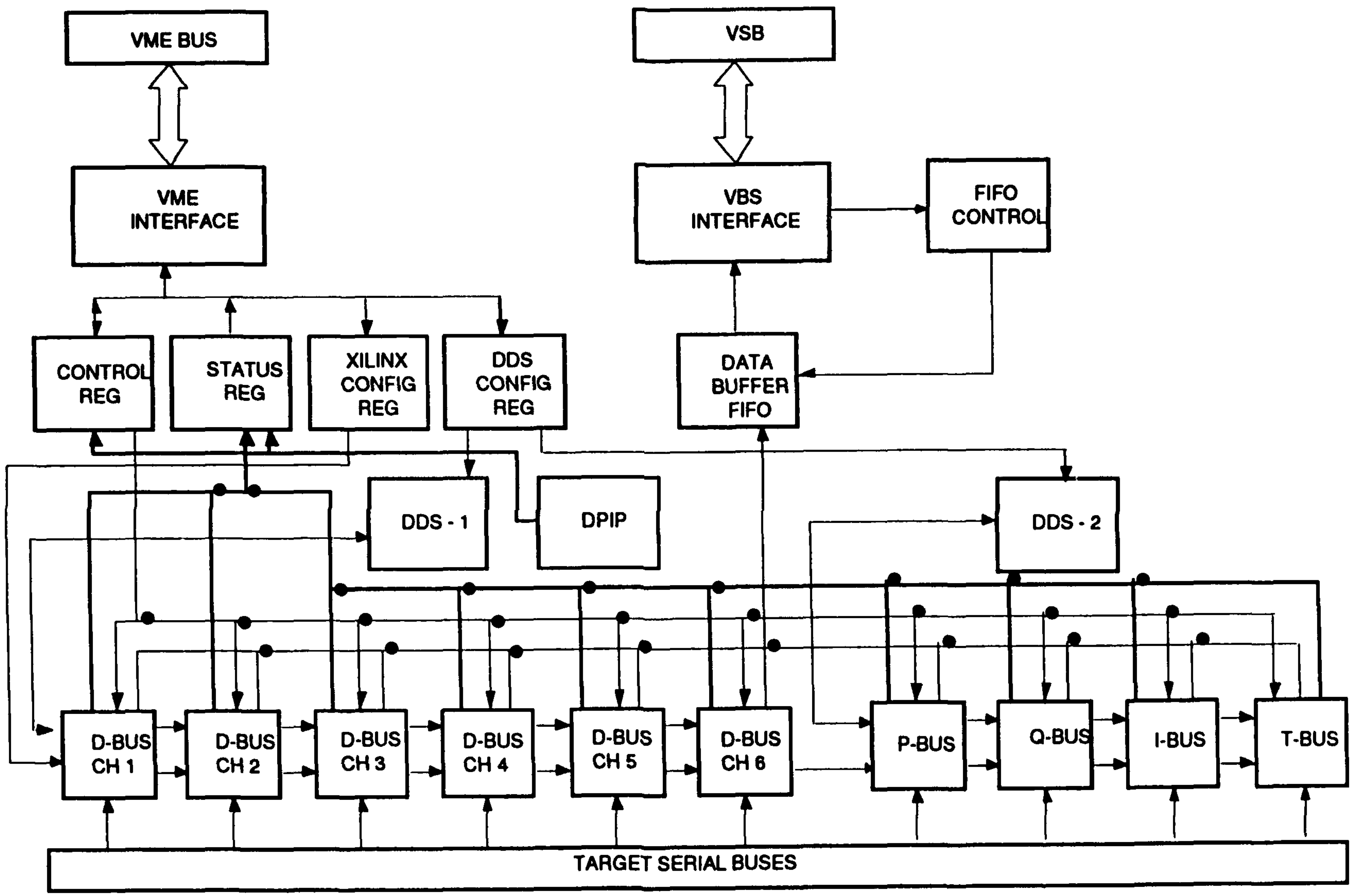


Figure 10-1. DICE Top Level Board Interconnects

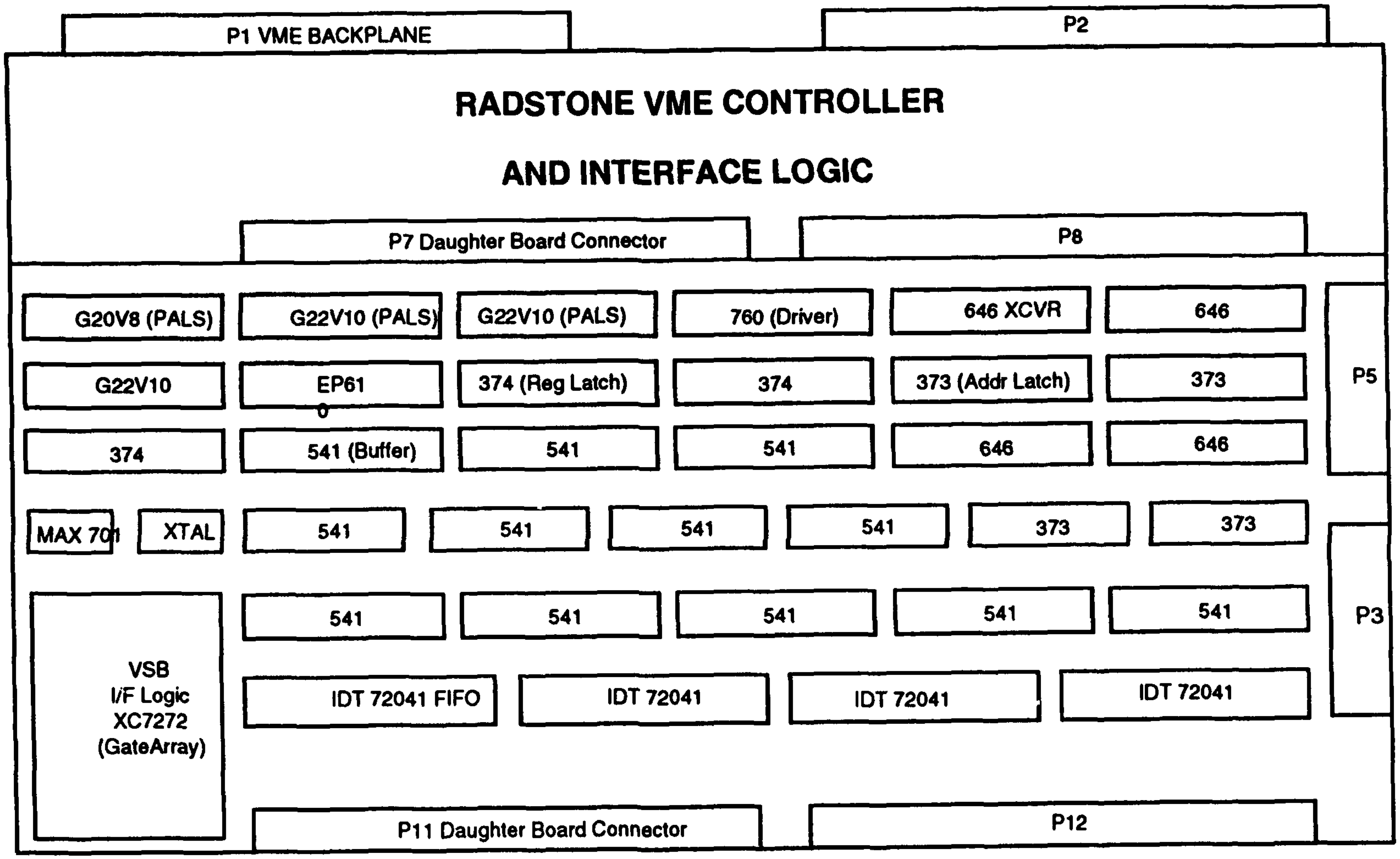


Figure 10-2. RADSTONE VP1 Development Board Block Layout

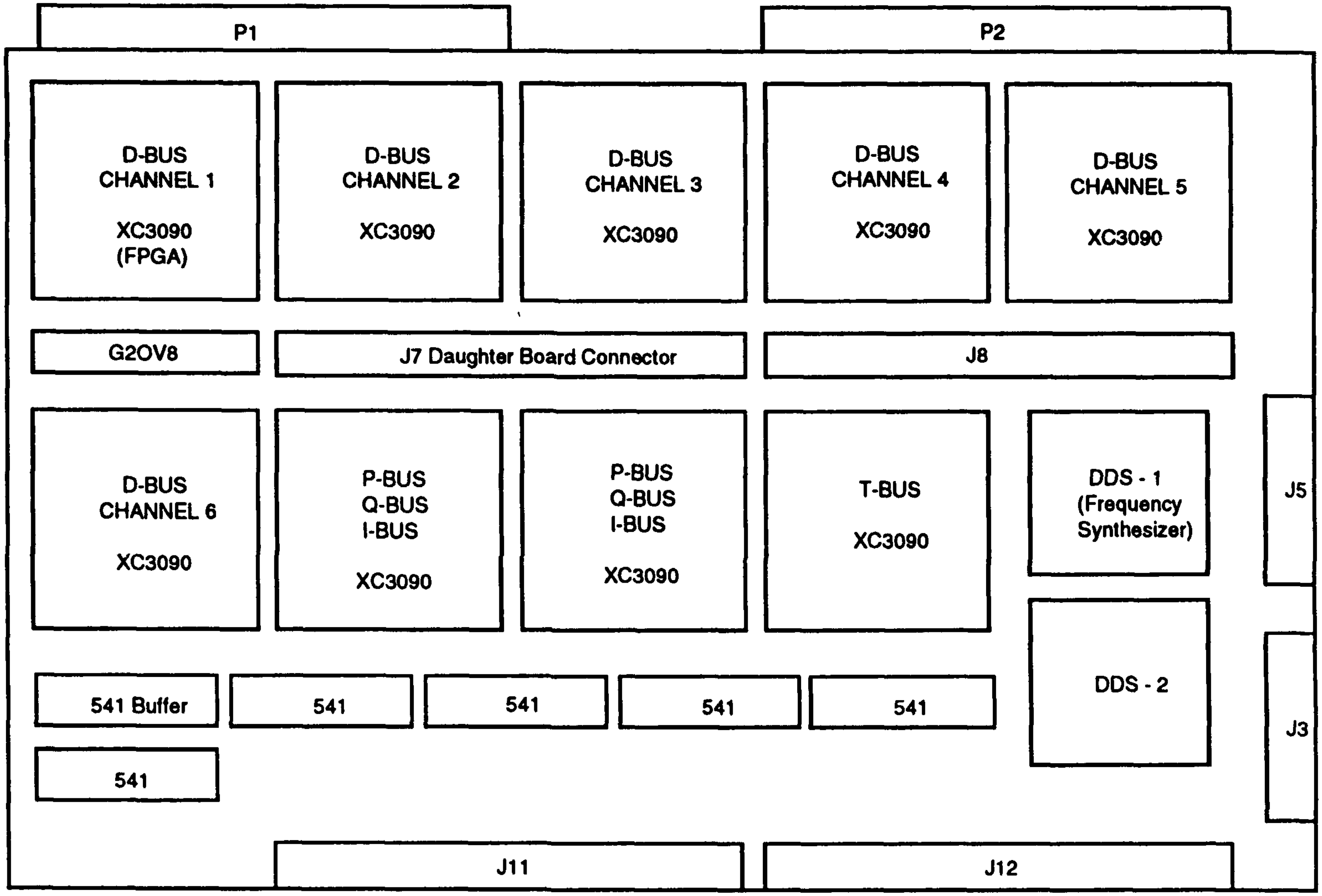


Figure 10-3. Custom 6U VME Interface Board Block Layout

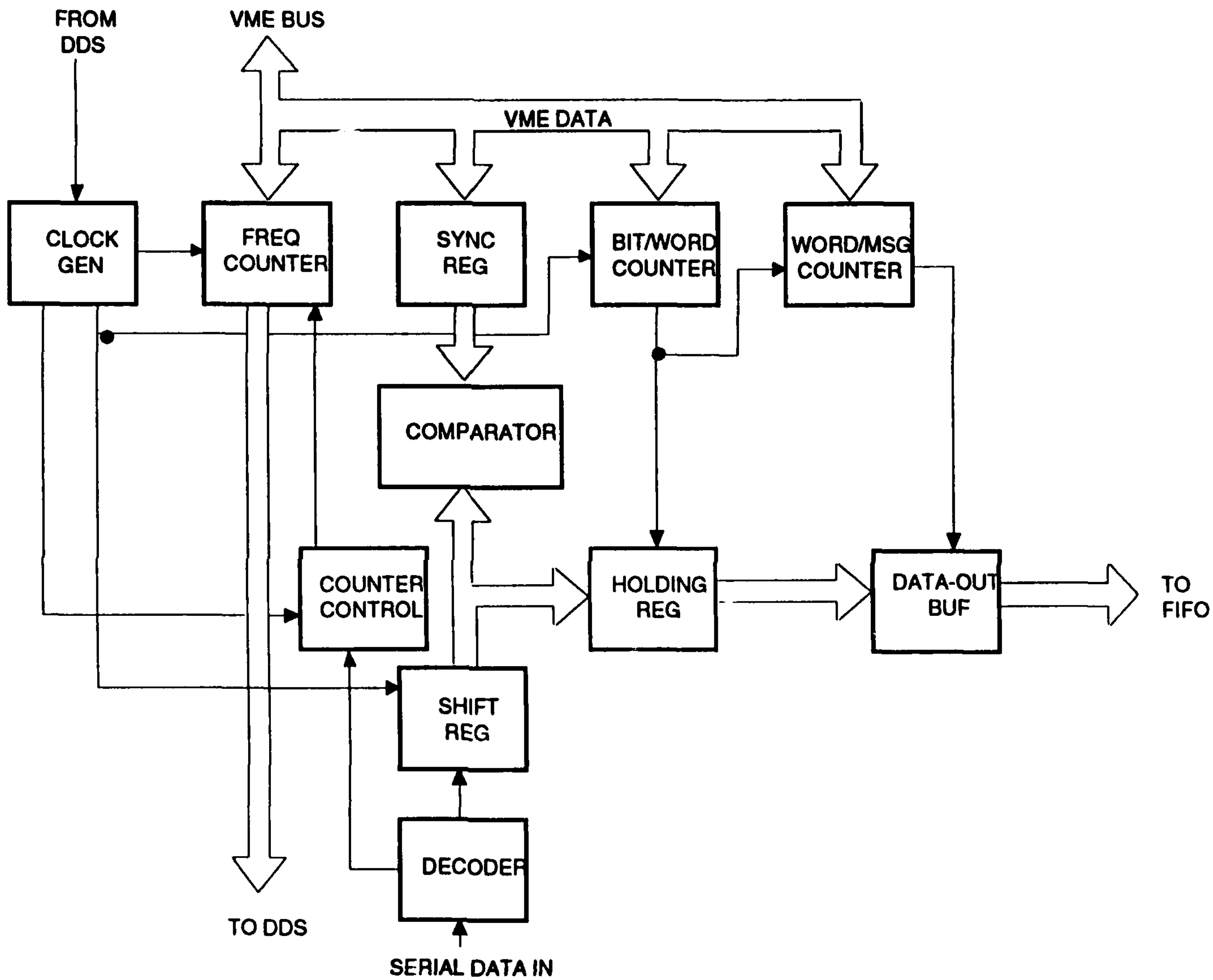
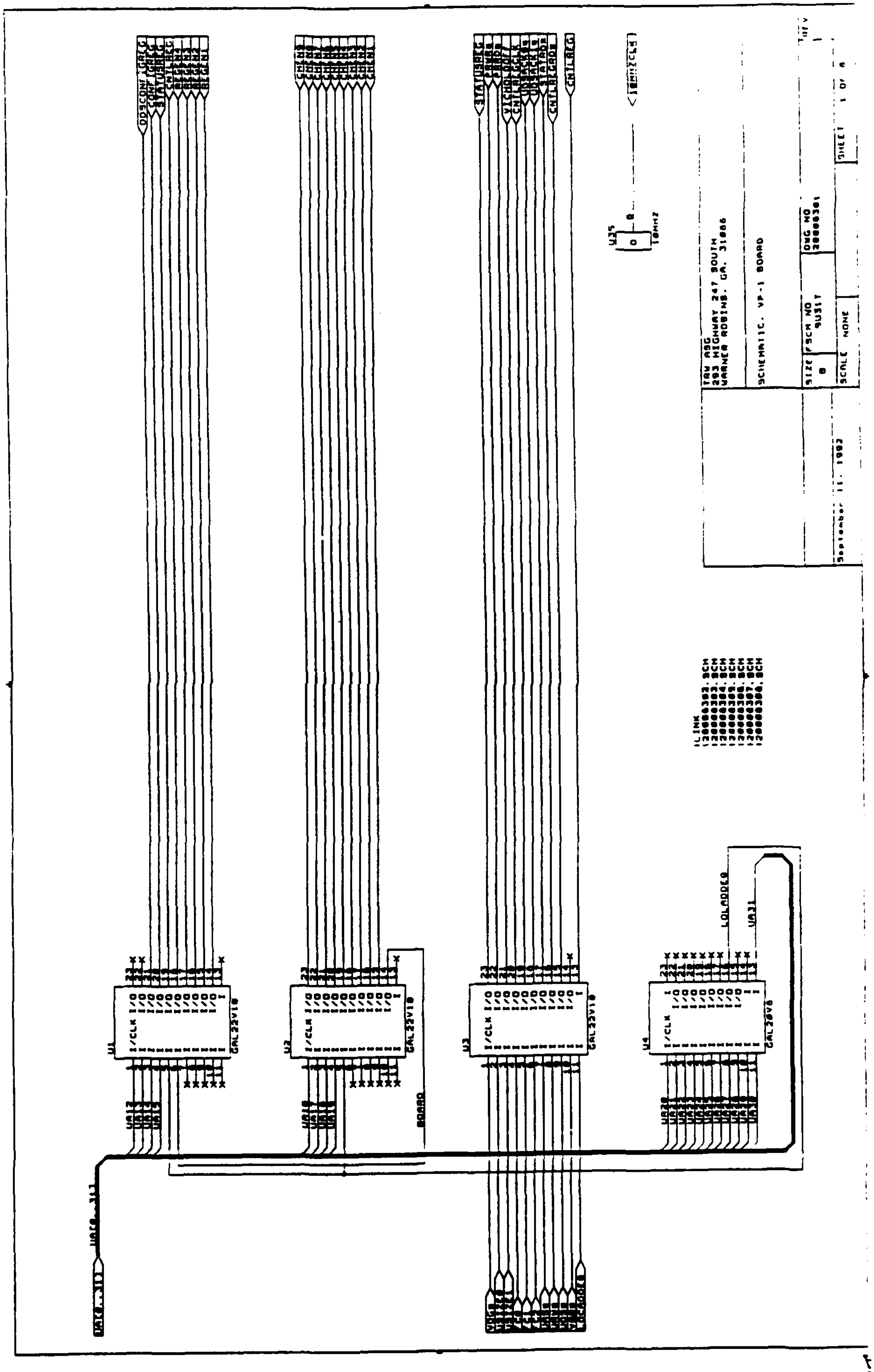
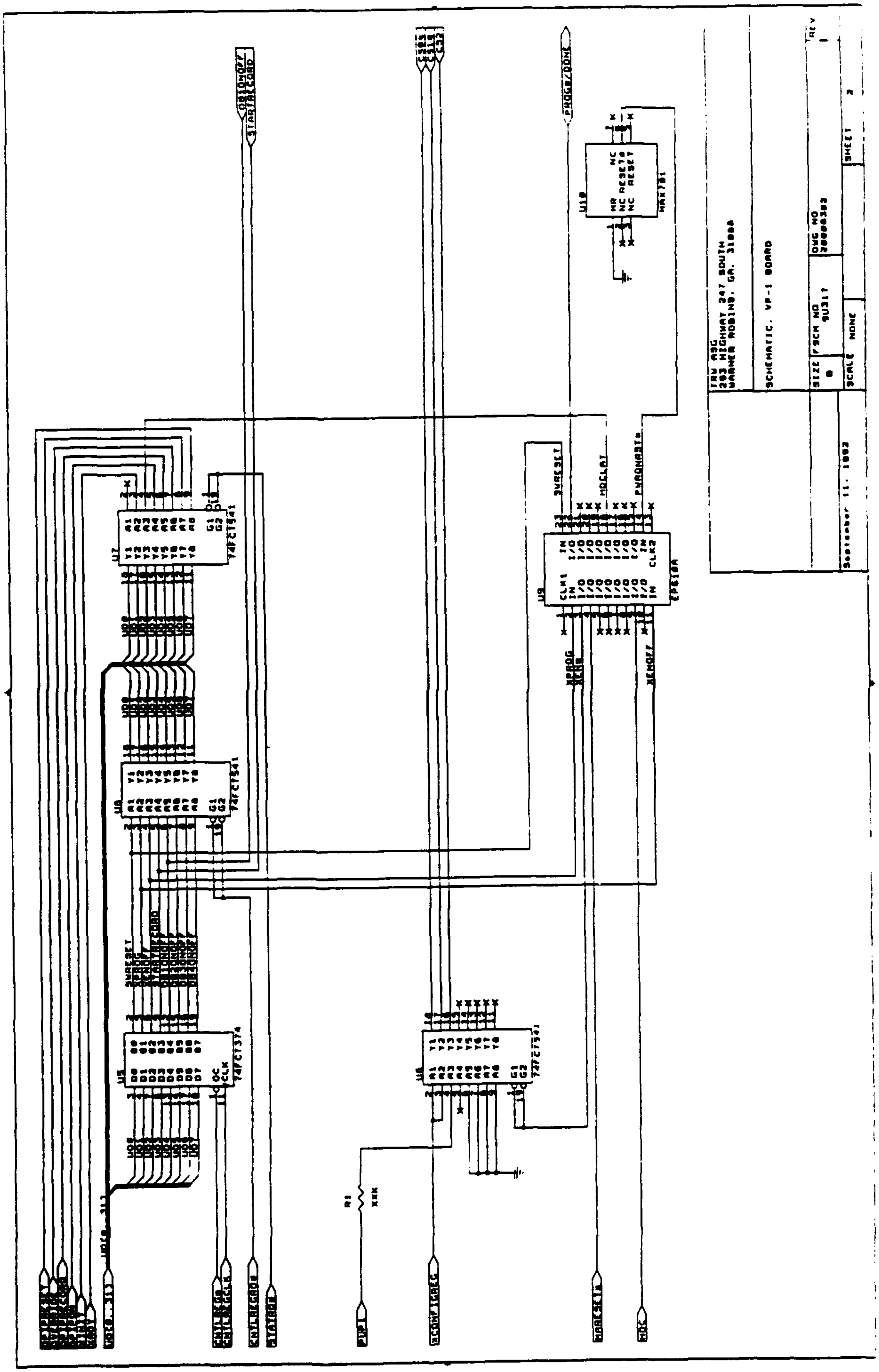
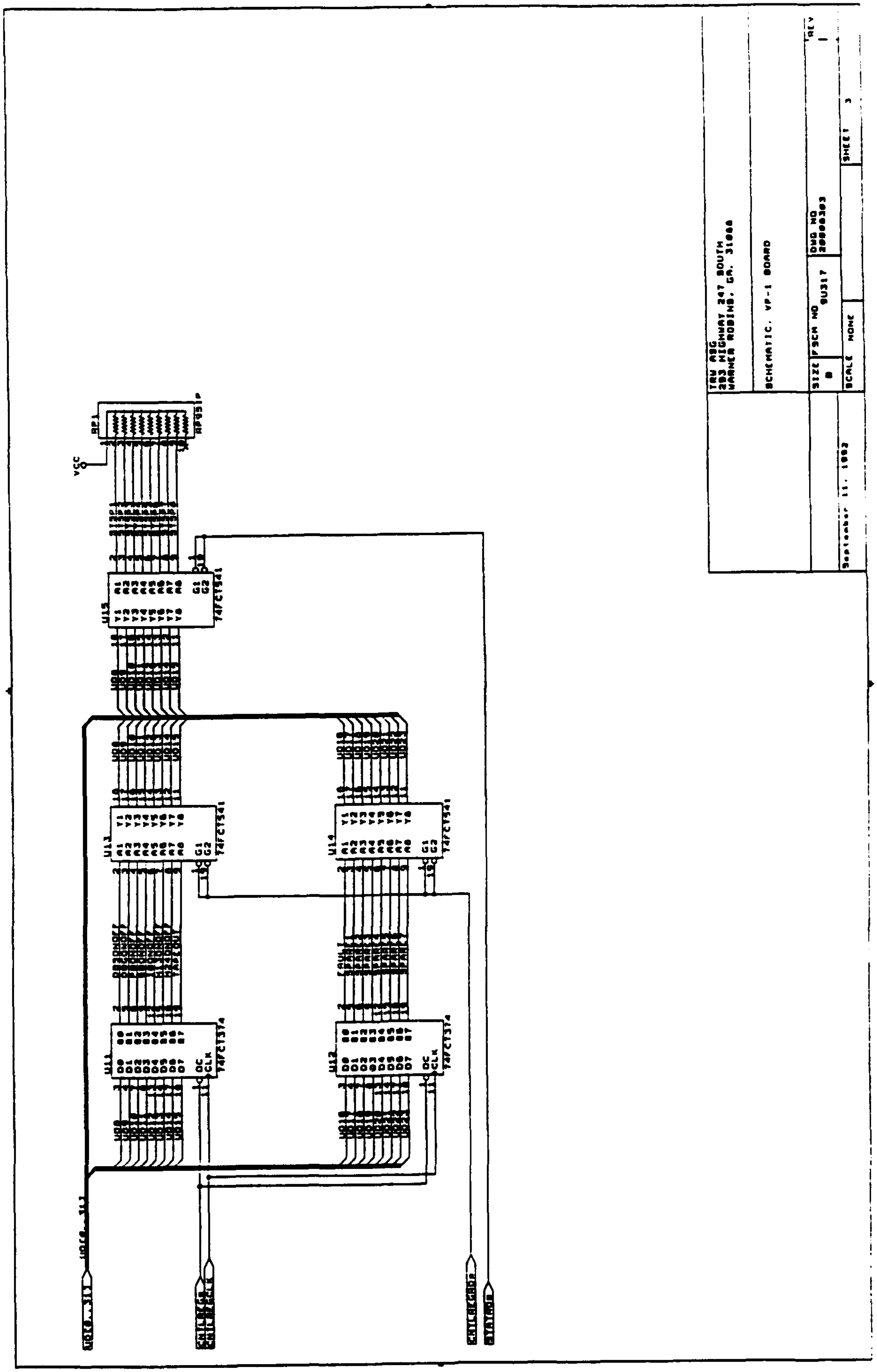


Figure 10-4. Sample Channel Process



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74FCT541
U13
74FCT541
U14
74FCT541
U11
74FCT374
U12
74FCT374
TRW ASG
283 HIGHWAY 247 SOUTH
WARNER ROBINS, GA. 31088
SCHEMATIC, VP-1 BOARD
SIZE
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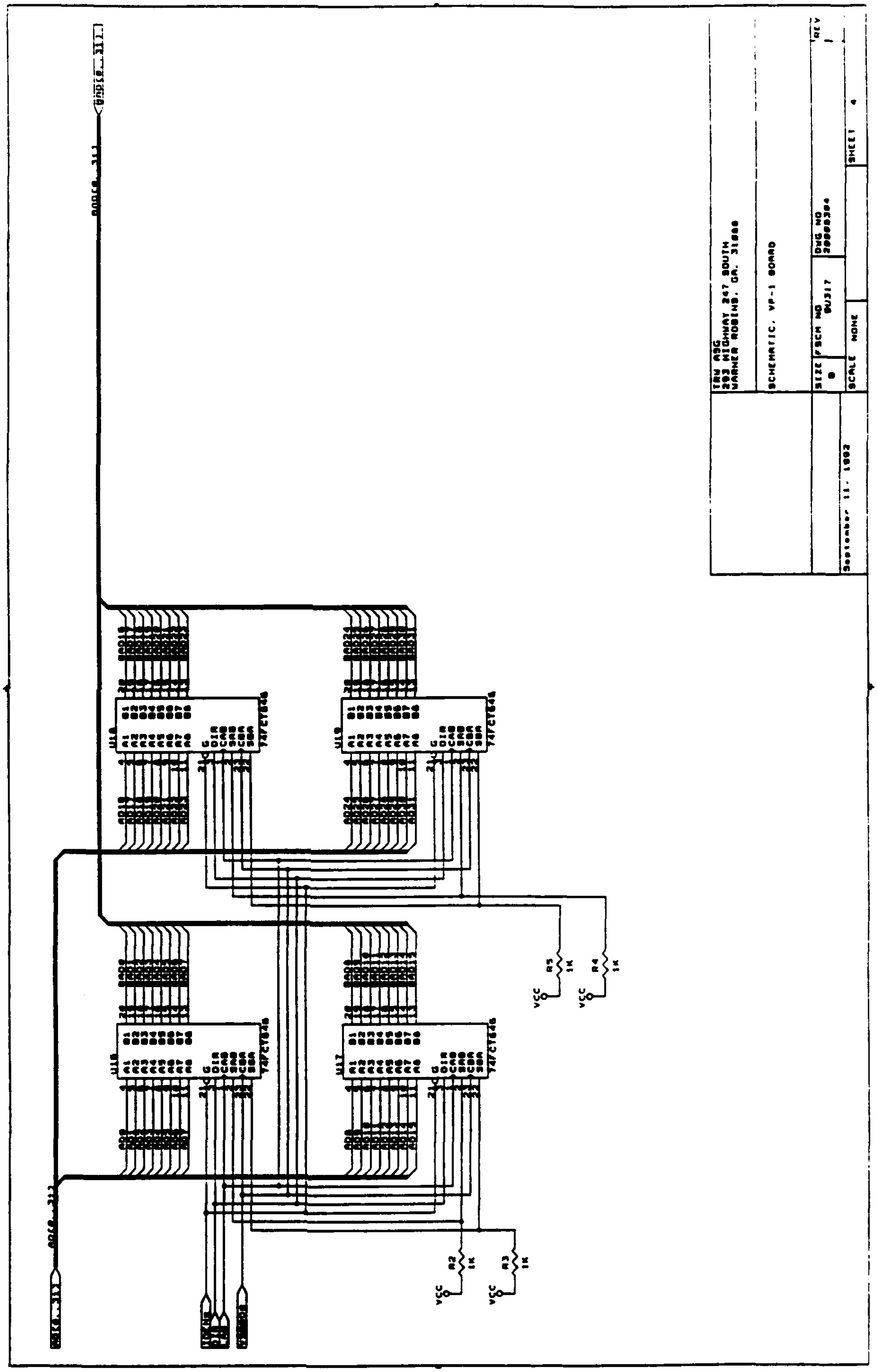
FSCM NO
9U317
DWG NO
SCALE
NONE
SHEET
3
REV
September 11, 1992


TRW ASG
293 HIGHWAY 247 SOUTH
WARNER ROBINS, GA.
SCHEMATIC, VP-1 BOARD
SIZE
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FSCM NO
DWG NO
REV
SHEET 4
SCALE NONE
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U18
U19
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R2
R3
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R5
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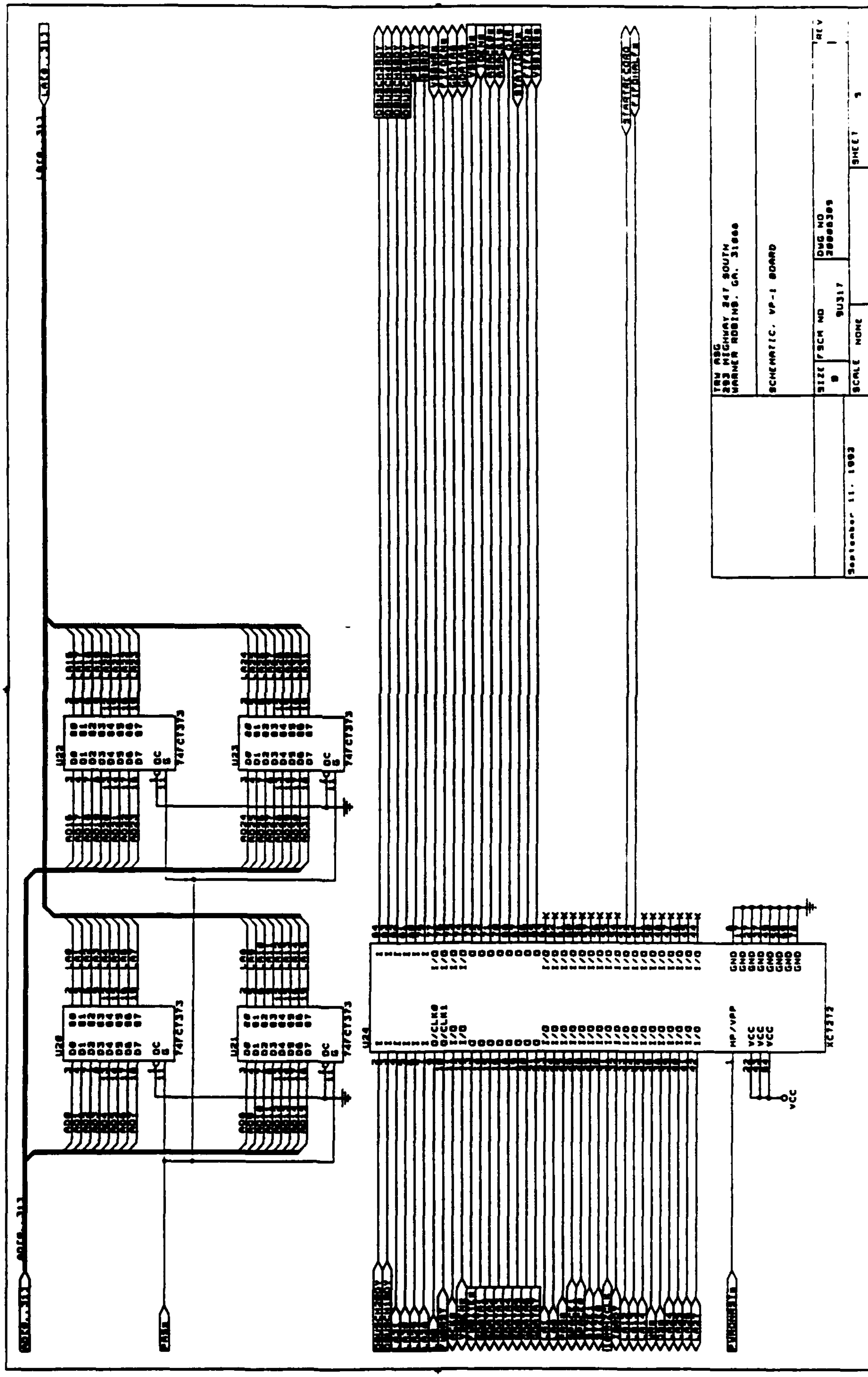

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U22
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WARNER ROBINS, GA. 31088
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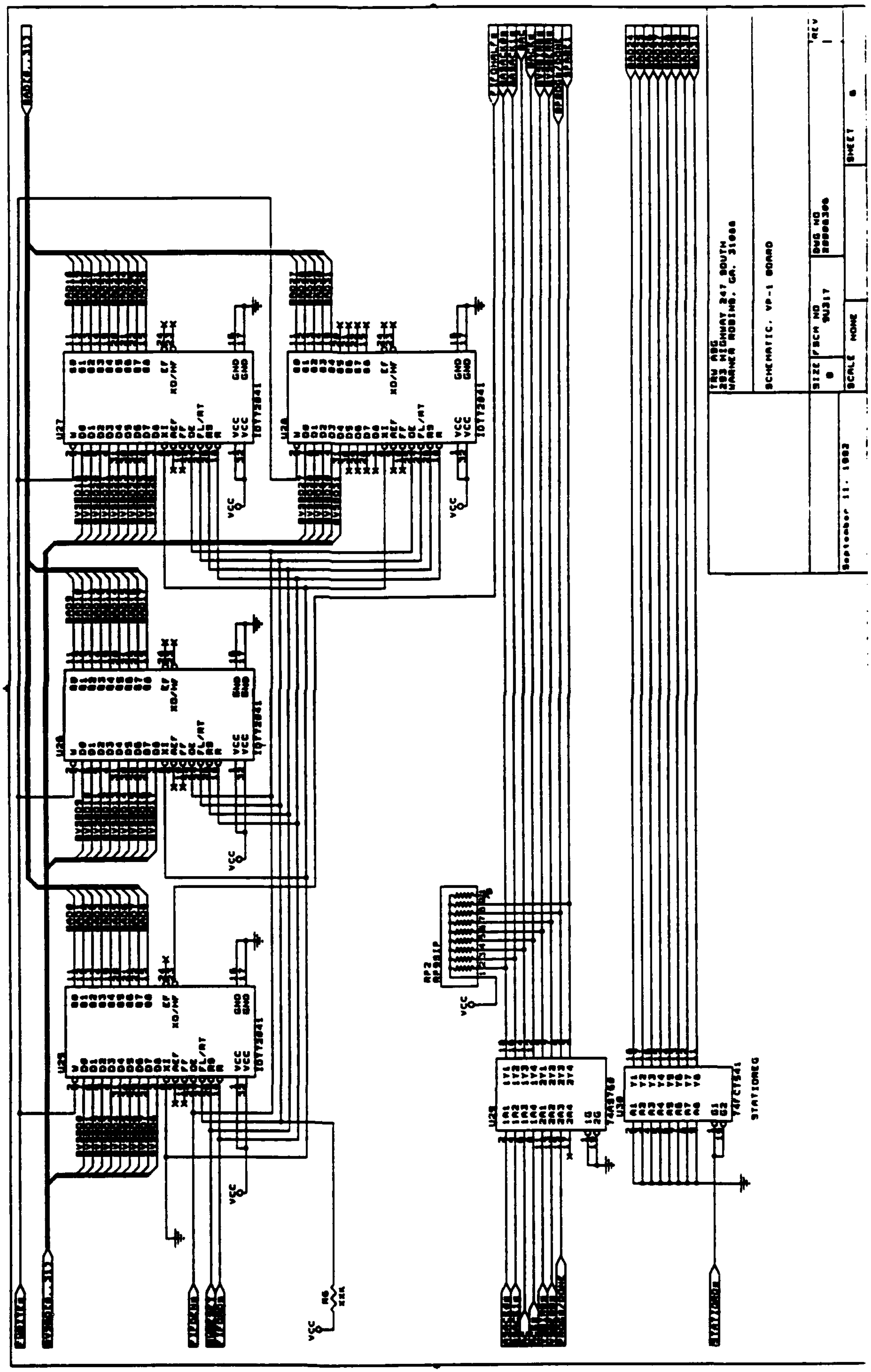

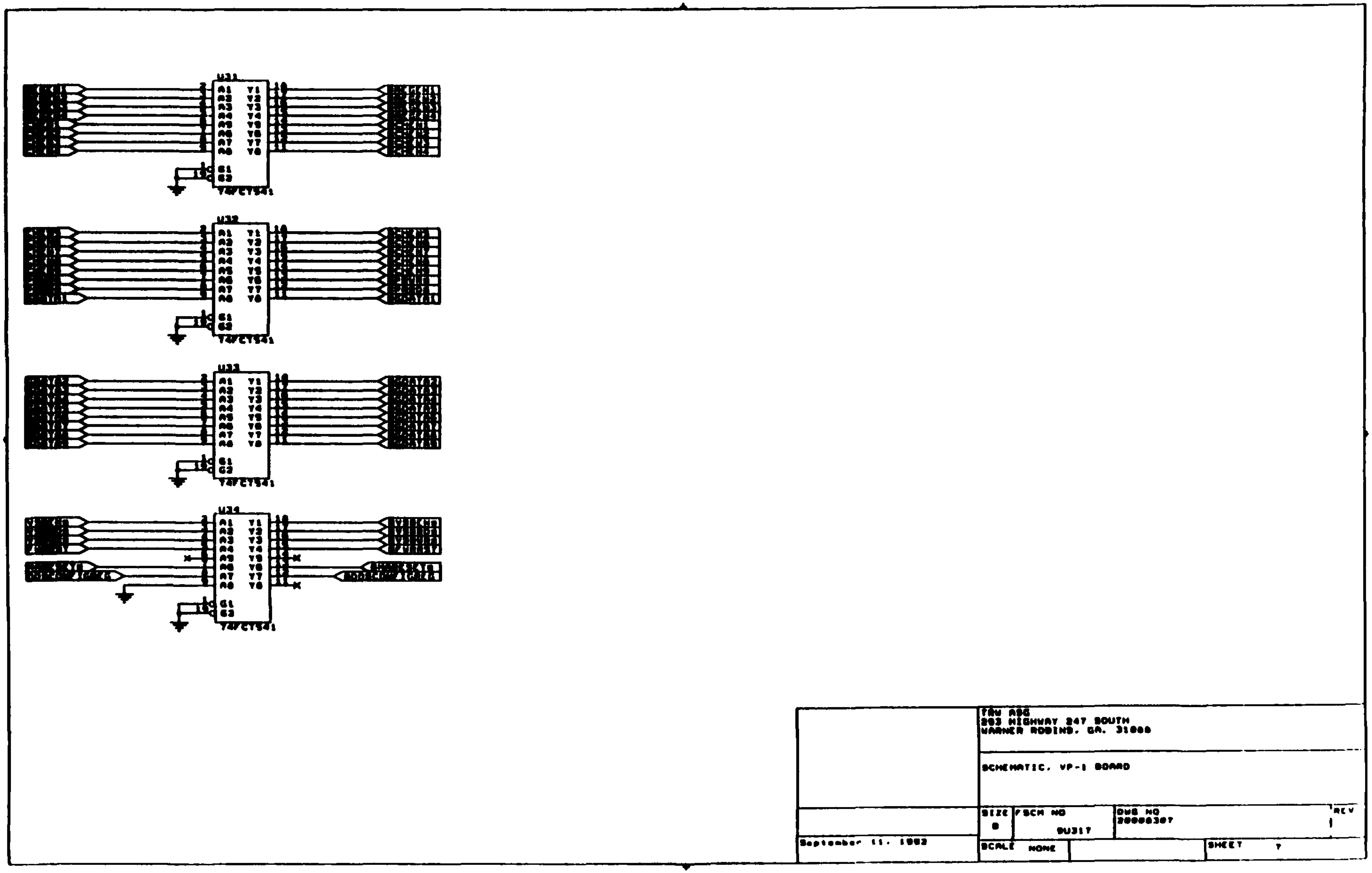
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U34
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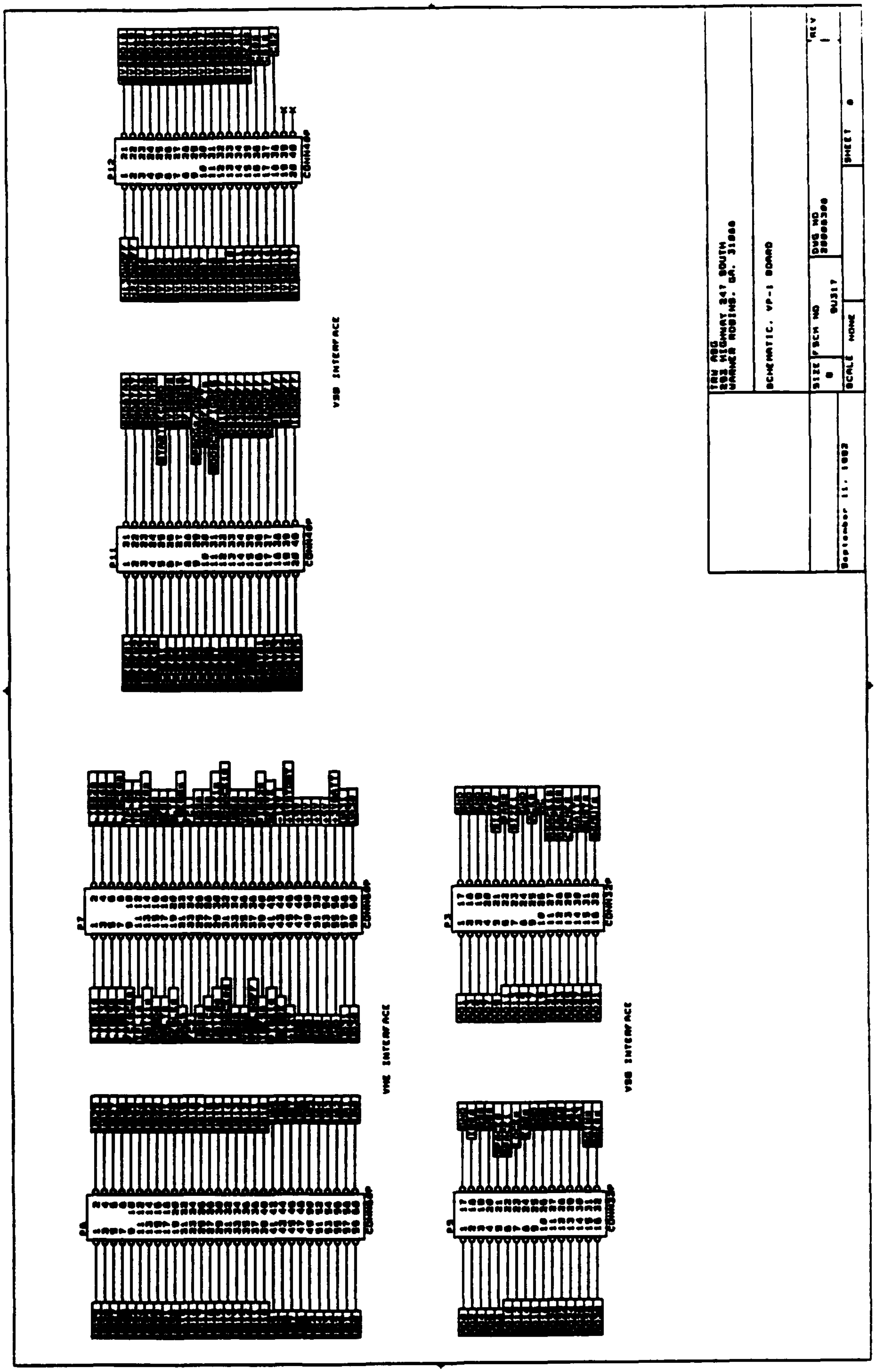

TRW ASG
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SCHEMATIC, VP-1 BOARD
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DWG NO
SCALE NONE
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REV
VSB INTERFACE
VME INTERFACE